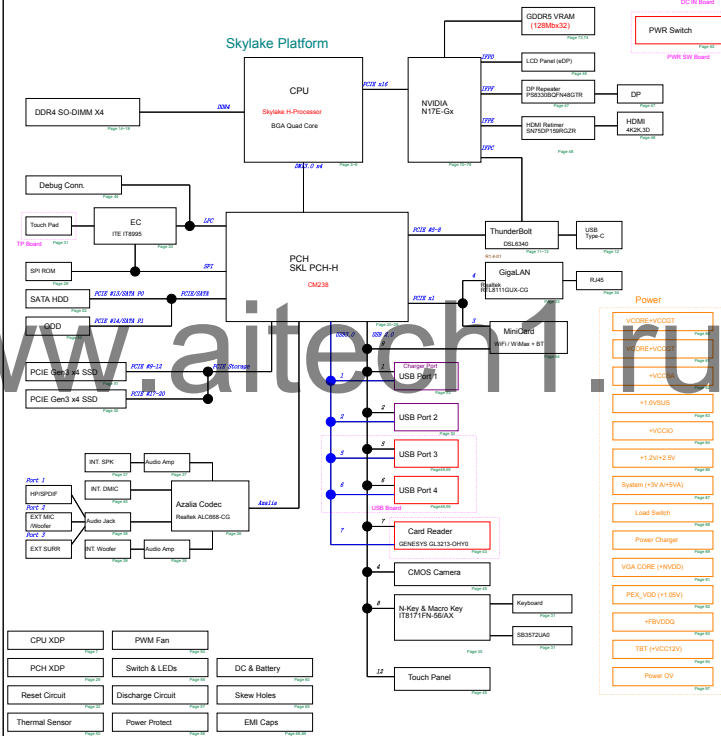


- [illegible]

## G752VSK Block Diagram



[illegible]

C.11865 GHIO				
Year	Month	Day	Time	Location
2018	1	1	12:00	1000000
2018	1	1	12:01	1000000
2018	1	1	12:02	1000000
2018	1	1	12:03	1000000
2018	1	1	12:04	1000000
2018	1	1	12:05	1000000
2018	1	1	12:06	1000000
2018	1	1	12:07	1000000
2018	1	1	12:08	1000000
2018	1	1	12:09	1000000
2018	1	1	12:10	1000000
2018	1	1	12:11	1000000
2018	1	1	12:12	1000000
2018	1	1	12:13	1000000
2018	1	1	12:14	1000000
2018	1	1	12:15	1000000
2018	1	1	12:16	1000000
2018	1	1	12:17	1000000
2018	1	1	12:18	1000000
2018	1	1	12:19	1000000
2018	1	1	12:20	1000000
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2018	1	1	12:22	1000000
2018	1	1	12:23	1000000
2018	1	1	12:24	1000000
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2018	1	1	12:31	1000000
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2018	1	1	12:37	1000000
2018	1	1	12:38	1000000
2018	1	1	12:39	1000000
2018	1	1	12:40	1000000
2018	1	1	12:41	1000000
2018	1	1	12:42	1000000
2018	1	1	12:43	1000000
2018	1	1	12:44	1000000
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2018	1	1	12:46	1000000
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2018	1	1	15:32	1000000
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2018	1	1	16:11	1000000
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2018	1	1	16:16	1000000
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2018				

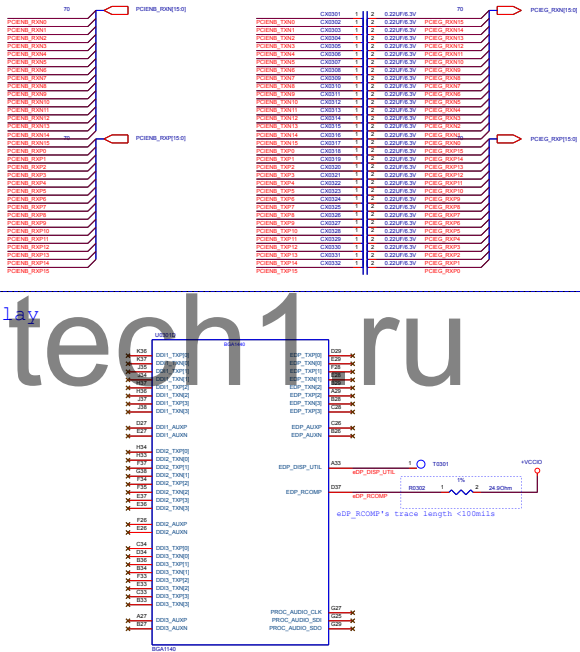
Course Identification		
Course Number/Name		
CR	000000-00000	000000-00
CR		
Student History Record		
CR	00000000000000000000	
CR		

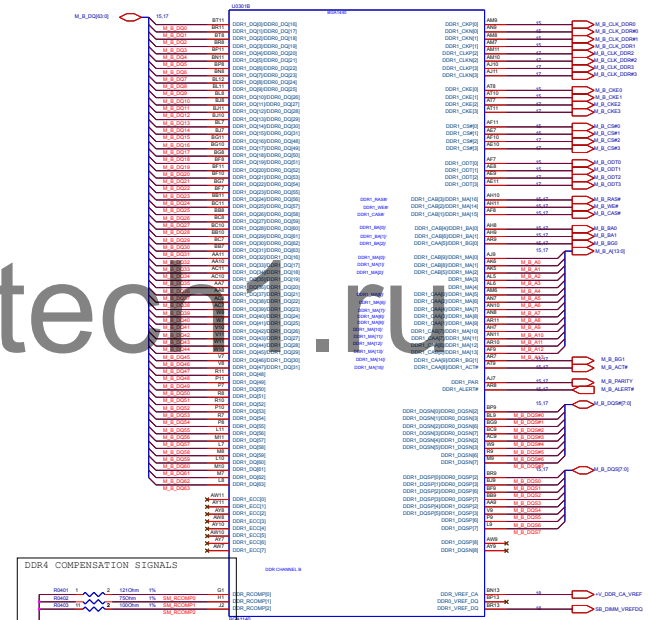
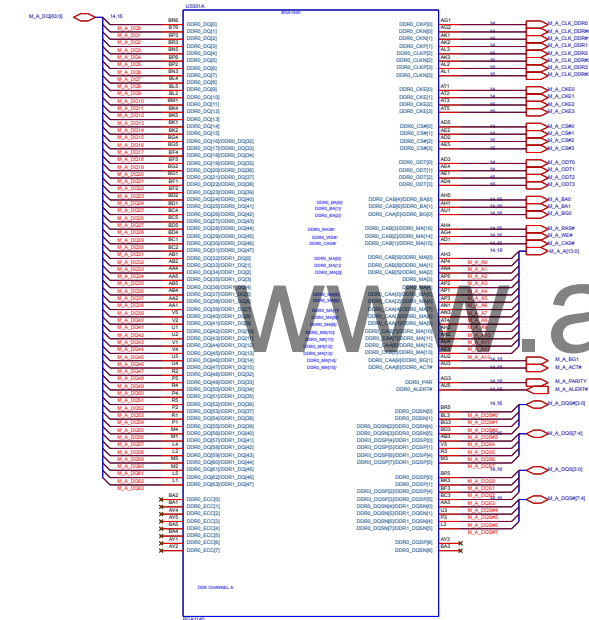
[illegible][illegible][illegible][illegible][illegible]

## DMI &amp; PCIEG



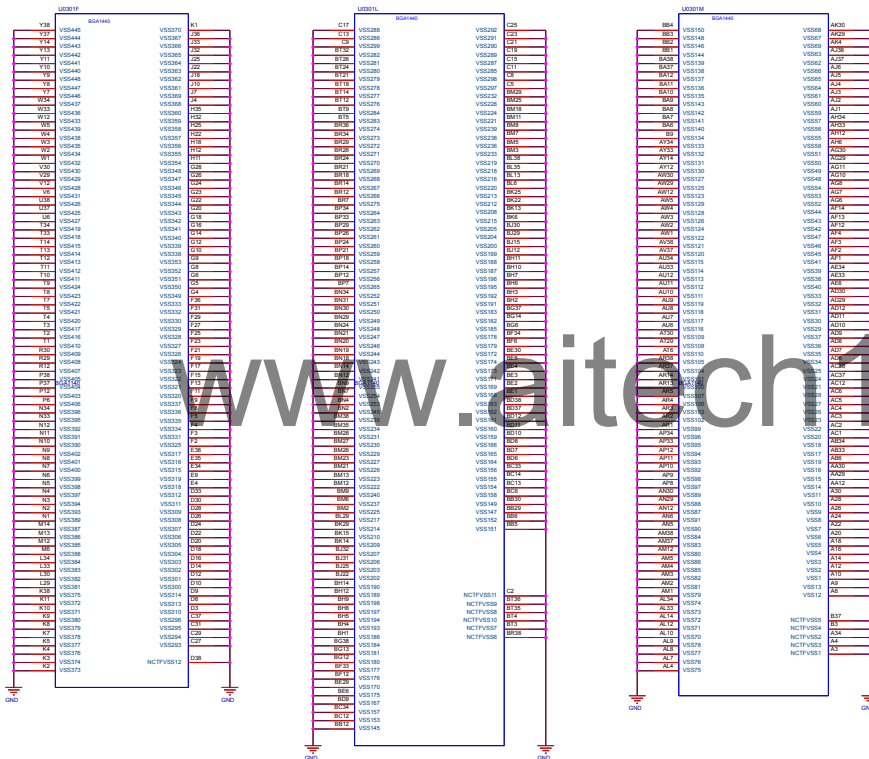
## Display





Main Board



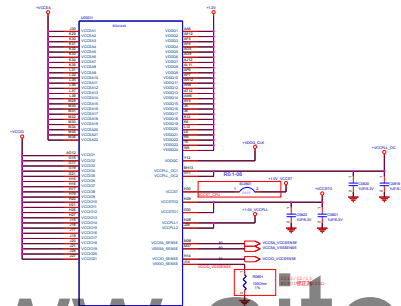




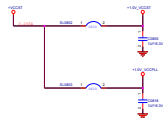
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# OPC Power Rails

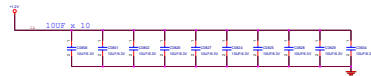
Main Board



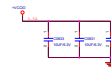
+1.0V\_VDDQST/+1.0V\_VDDQPL  
DECAPS Place Back Side (TOP)



+VDDQ DECAPS Place Back Side (TOP)



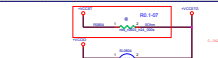
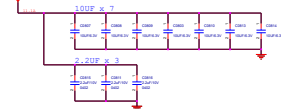
+VDDQ DECAPS Place Back Side (TOP)



+VDDQ\_CLK DECAPS Place Back Side (TOP)

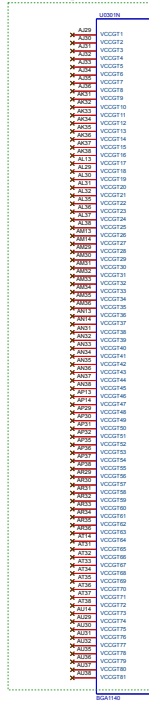


+VDDQ DECAPS Place Back Side (TOP)



Volume Segment  
+VDDQ is supplied +1.0V (shared with +VDDQSTG)

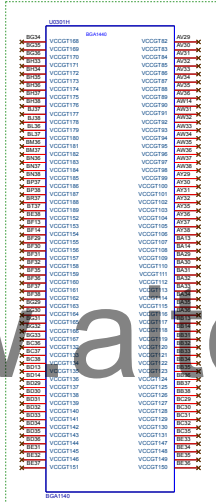
For MS-Hybrid



For W/GT3/GT4 CPU



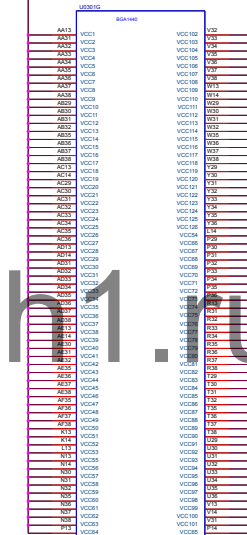
For MS-Hybrid



For MS-Hybrid



+VCCCORE

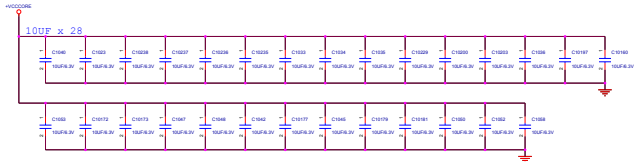


+VCCCORE

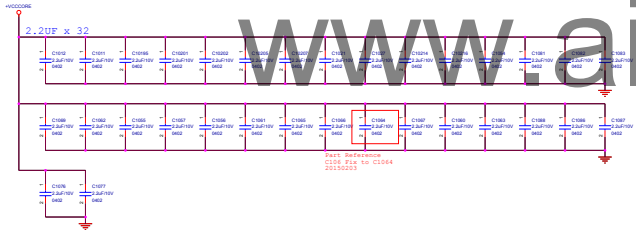


Main Board

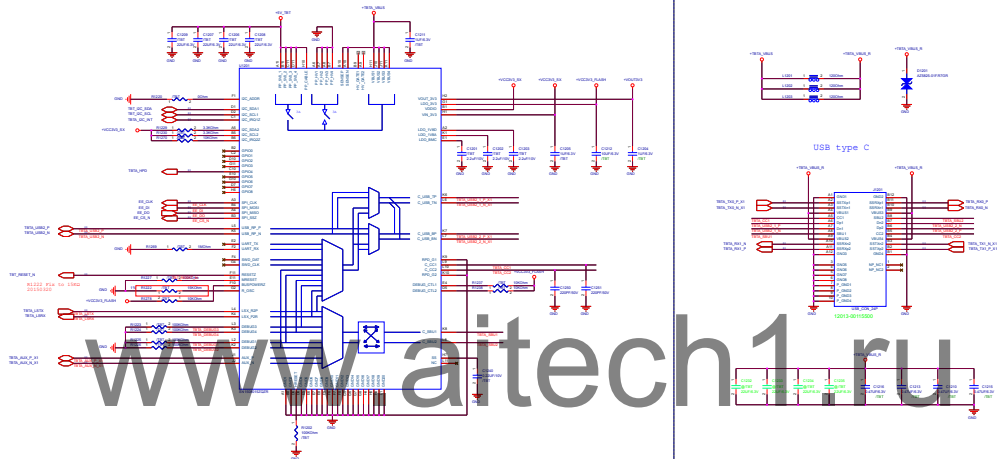
+VCCORE DECAPS Place Back Side (TOP)



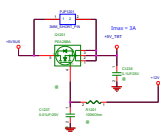
+VCCGT DECAPS Place Back Side (TOP)



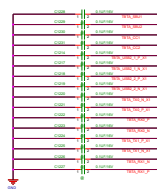




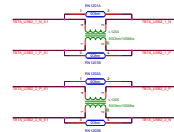
TBT 5V Power

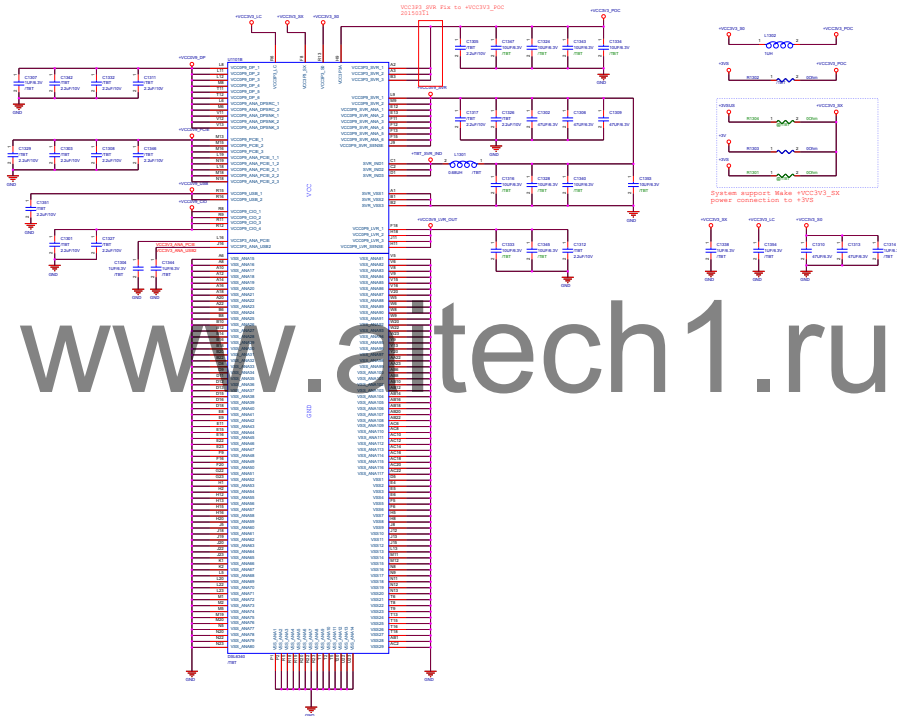


ESD-Protection



20161011 AGO ESD on high speed lines

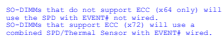




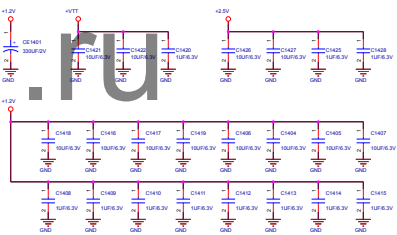
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12002-00080600  
DDR4 DIMM 260P 4H REV



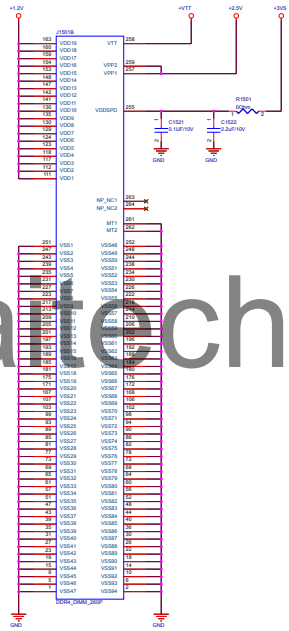
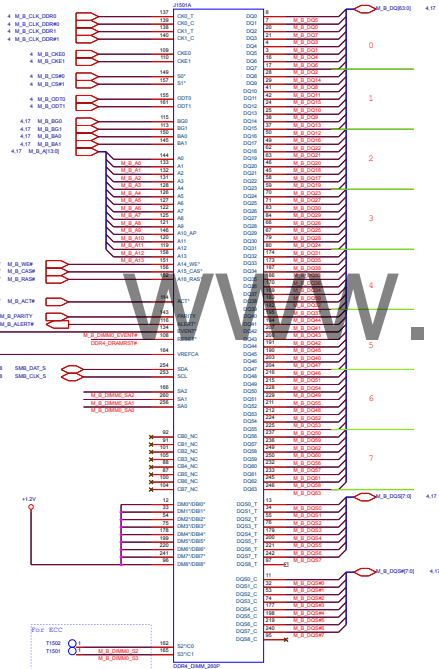
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREPCA (0.6V From +1.2V)
	+3VA_DSX	+3VS
		+2.5V

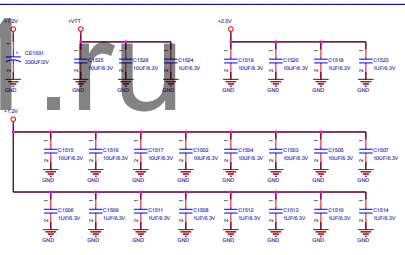
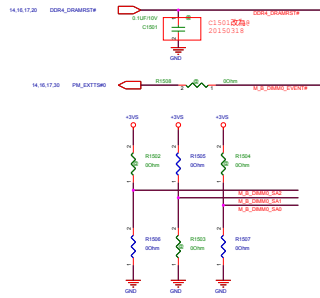
SODIMM CHB-DIMM0  
TOP H4.0mm STD (J1501)

12002-00080700  
DDR4 DIMM 260P 4H STD



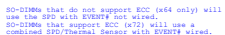
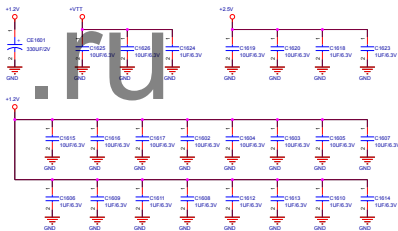
SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.  
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



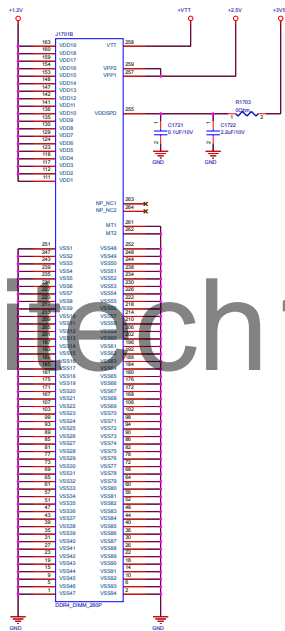
Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From FUS600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

12002-00080700  
DDR4 DIMM 260P 4H STD

[illegible]

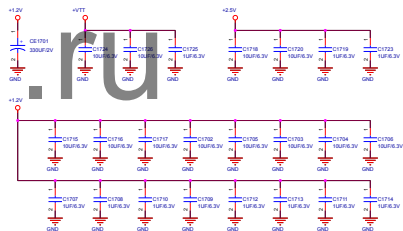
Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From FUS600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

12002-00080500  
DDR4 DIMM 260P 8H STD



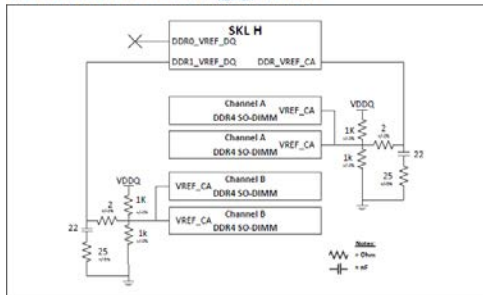
SO-DIMMs that do not support ECC (x64 only)  
will use the SPD with EVENT# not wired.  
SO-DIMMs that support ECC (x72) will use a  
combined SPD/Thermal Sensor with EVENT# wired.

EVENTS ON ECC DIMM: KEEP A PULL UP IF NO PIN IN BCH

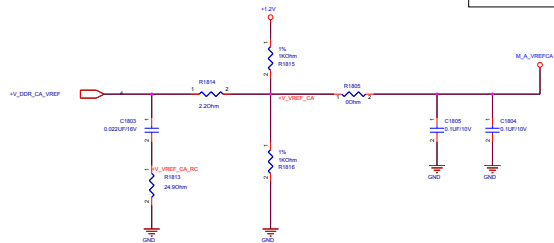


		Project Name <b>G752YSK</b>	Rev <b>R2.0</b>
Title : <b>DIM_DDR4 SO-DIMM B0</b>			
Size Custom	Dept.: <b>ASUSTEK COMPUTER INC.</b> Engineer: <b>Ashton_yang</b>		
Date: <b>Wednesday, October 12, 2016</b>		Sheet <b>17</b> of <b>102</b>	

# SKL H DDR4/DDR4-RS SO-DIMM V<sub>REF-CA</sub> Overview



SO-DIMM Vref



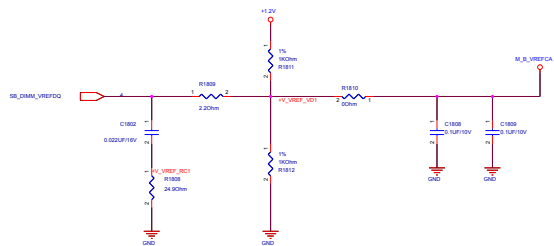
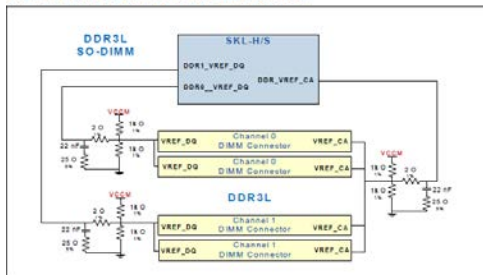
Main Board

Main Source	1th PWR	2nd PWR
AC_SNS_VSB	+1.2V	MAX VREF-CA (0.0V From +1.2V)

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SO-DIMM Vref

## SKL H and SKL S DDR3L SODIMM VREF Overview

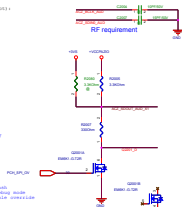


The screenshot shows a table with 4 columns: Pin Name, Pin Number, Pin Type, and Pin Description. The rows are as follows:

Pin Name	Pin Number	Pin Type	Pin Description
AC2_ICLA_AUG	1	IO	AC2_ICLA_AUG_A1
AC2_EVNC_AUG	2	IO	AC2_EVNC_AUG_A1
AC2_AUG_AUG	3	IO	AC2_AUG_AUG_A1
AC2_SDOCT_AUG	4	IO	AC2_SDOCT_AUG_A1

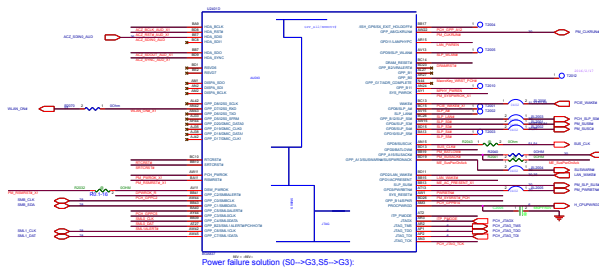
Below the table, there is a note: "NDA JTAG (On-Die JTAG via voltage select): N/A (Edge of 3000000000 Hz) High: 1.5V, Low: 1.0V (default)".

NDA\_FUNC(Co-Die PLL VR voltage select):  
Rising edge of NDAOUT0 pin  
High:1.5V, Low:1.5V (default)

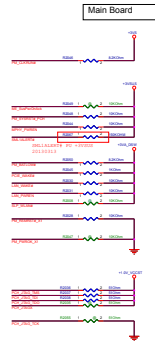


```
ACE_SDOOT:
(1)PCW:
Internal PD 20k ohm,
VIL<0.35V,VIH>0.65-1.3V
(2)ALC269:
VIL<0.35*1.3V,VIH>0.65*1.3V
```

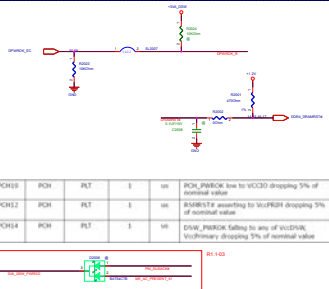
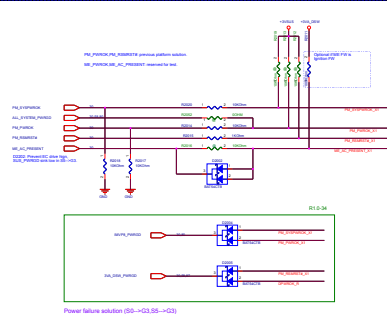
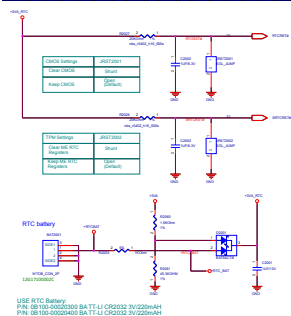
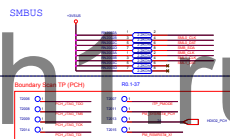
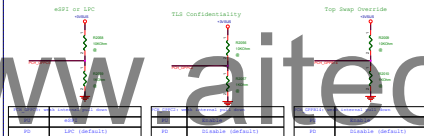
ACE IDONT is a signal used for Flash Descriptor security Override/NE Debug mode  
NICE : set overrides, LOW : disable override

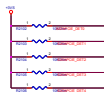


Power failure solution (S0→G3,S5→G3):

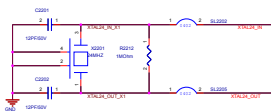


Main Source	1th FMS	2nd FMS	3rd FMS	4th
+HSCB&T	+HSCB_S&T	+20A_S&T		
AC_S&T_SVS	+1.0VDD08	+VDD08	+1.0V_VDD08	
	+1.2V			
	+VDD06	+20A	+VDD06	
	+20A_S&W	+3VDD05	+VDD05+VDD04	+HSCPA120
		+3V05		

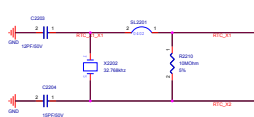


[illegible]

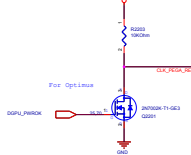
XTAL 24MHz



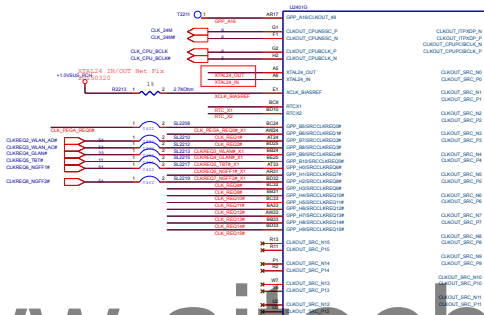
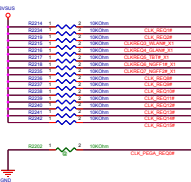
RTC CRYSTAL 32.768KHz



DGPU CLKReq#



PCH CLKREQ Setting:

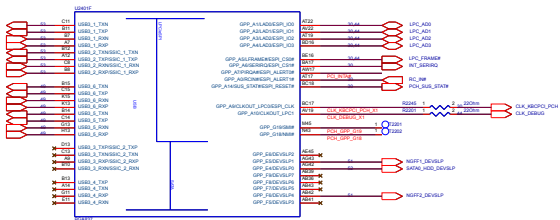


USB10 Port1 : J5001

USB10 Port2 : N/A

USB10 Port4 : J5002

USB10 Port5 : J5001



PCH

XDP

100

MHz

VGA

330

MHz

PCIEX2

WLAN\_AD

PCIEX4

WLAN\_AC

PCIEX4

GLAN

PCIEX5-8

TDRout

PCIEX9-12

NGFF1

PCIEX17-20

NGFF2

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

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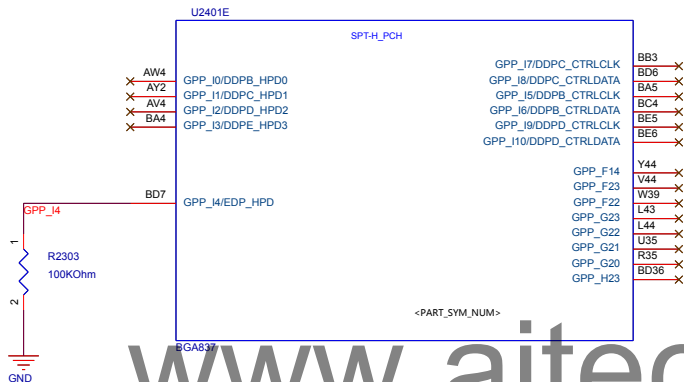
CLK\_REQ#

CLK\_REQ#

CLK\_REQ#

CLK\_REQ#




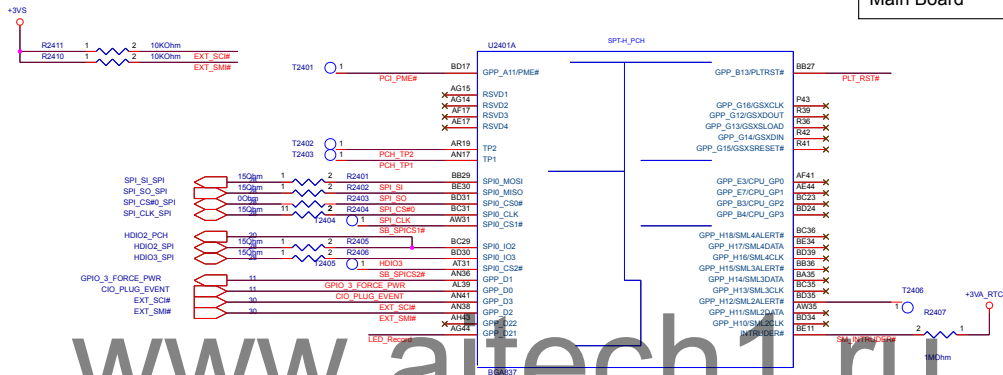


DDPD Strap Setting Update :  
 0 = Port D is not detected (Default)  
 1 = Port D is detected  
 20150309

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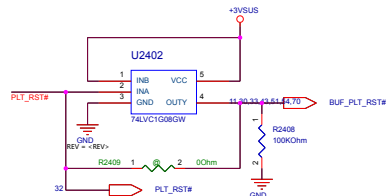
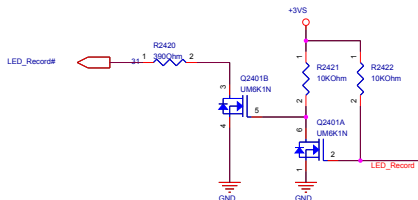
REV = <REV>

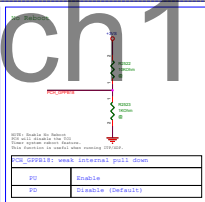
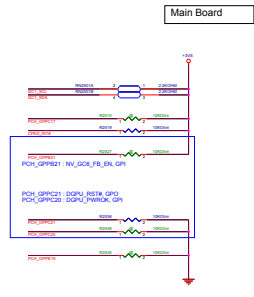
		Project Name	Rev
		G752VSK	R2.0
Title : PCH-CPT(4)_CPT,PCI,DP			
Size	Dept.:	Engineer:	
A	ASUSTek COMPUTER INC.	Ashton_yang	
Date:	Wednesday, October 12, 2016		Sheet
			23 of 102



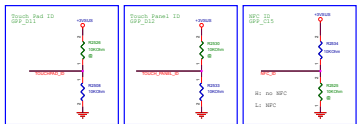
## Record Key LED Control Circuit

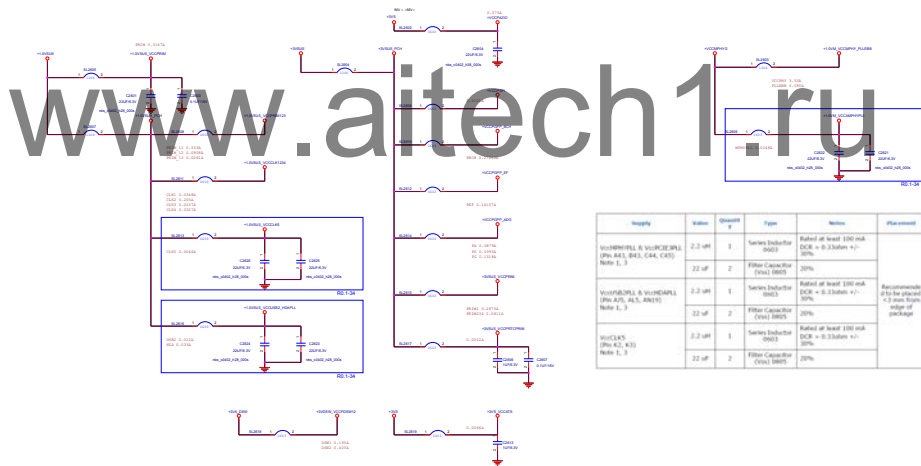
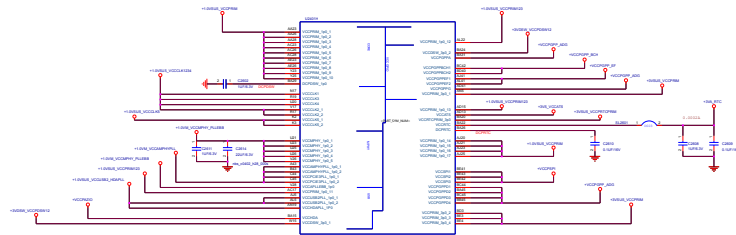
LED Record# of Current :  
 $(5-2.35) / 390 = 6.8\text{mA}$





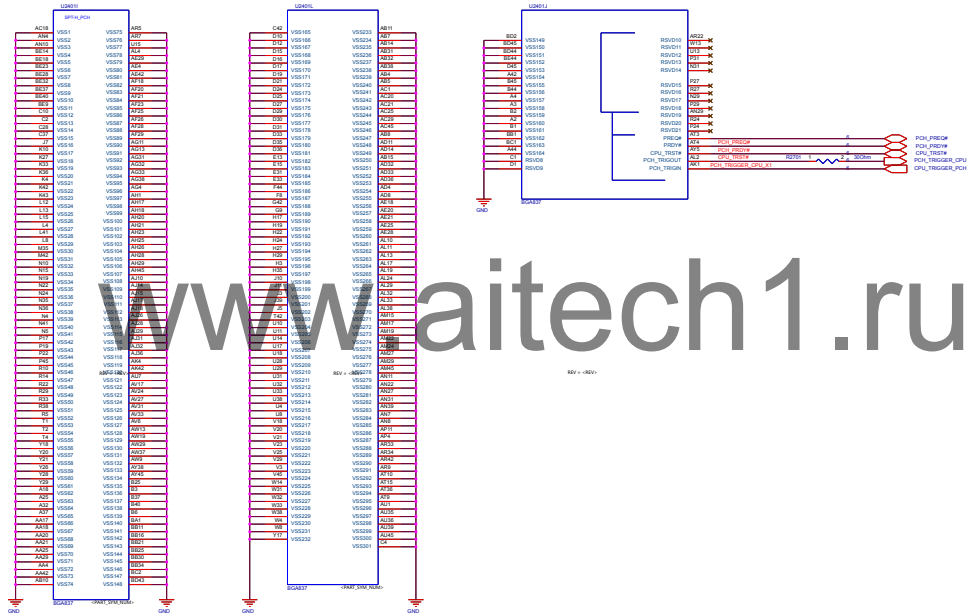
	PCR_ID0	PCR_ID1
Disable GC6	L	L
Enable GC6	L	R



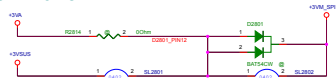


Supply	Value	Quantity	Type	Notes	Placement
VCCMIOPLL & VCCPCIEPLL (Pin A43, B43, C44, K45) Note 1, 3	2.2 uH	1	Series Inductor (0805)	Rated at least 100 mA, DCR = 0.33 ohms +/- 10%	Recommend to be placed within +/- 3 mm from edge of package
	22 uF	2	Filter Capacitor (C10A) 0805	20%	
VCCMIOPLL & VCCMIOPLL (Pin A43, B43, K45) Note 1, 3	2.2 uH	1	Series Inductor (0805)	Rated at least 100 mA, DCR = 0.33 ohms +/- 10%	
	22 uF	2	Filter Capacitor (C10A) 0805	20%	
VCCCKTS (Pin A2, K45) Note 1, 3	2.2 uH	1	Series Inductor (0805)	Rated at least 100 mA, DCR = 0.33 ohms +/- 10%	
	22 uF	2	Filter Capacitor (C10A) 0805	20%	

## Main Board

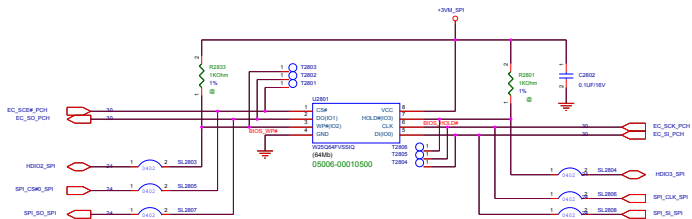


## SPI Power

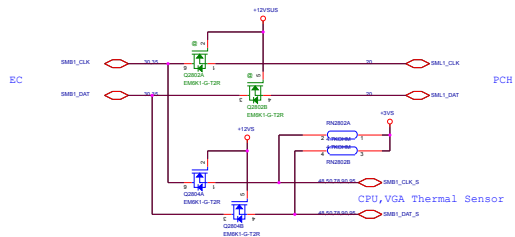


## 1st SPI ROM

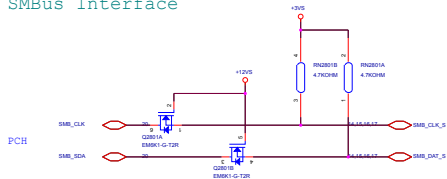
Main: 05006-00010500 (fixed quad bit)



## System Management Interface



## SMBus Interface



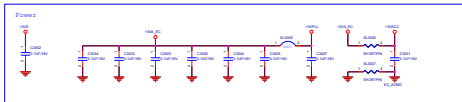
EC 8995

Only 3V Tolerance  
 GP0[0,1,2,3,4,5,6]  
 GP0[7,8,9,4,5,6,7]  
 GP0[0,4,5,6,7]  
 GP0[8]  
 GP0[7]  
 GP0[0,17]  
 GP0[0,17]  
 GP0[0,17]

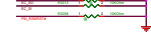
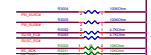
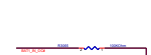
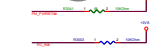
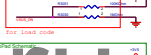
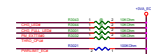
Can be adjusted to  
 Open-drain for pull

GP00-GP03  
 GP00-GP07  
 GP00-GP07  
 GP00-GP07  
 GP00-GP06  
 GP00-GP06  
 GP00-GP03

EC Inquire

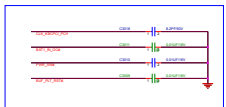
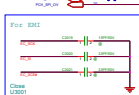
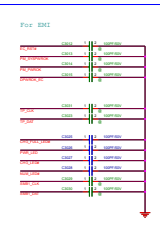


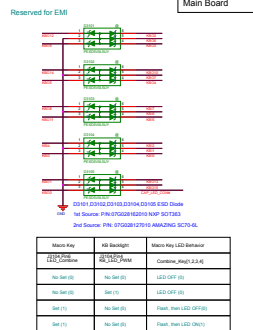
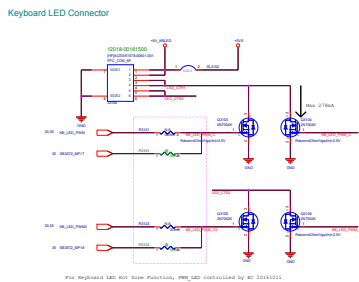
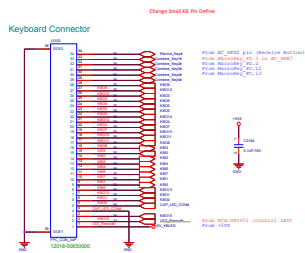
Main Board



EC Version	GP0 0
17889500-120/12	17889500-120/12
17889500-120/12	17889500-120/12

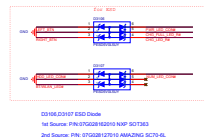
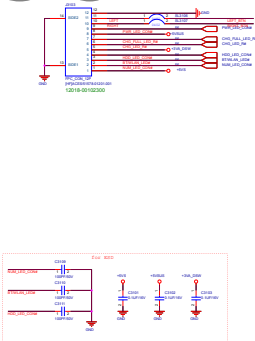
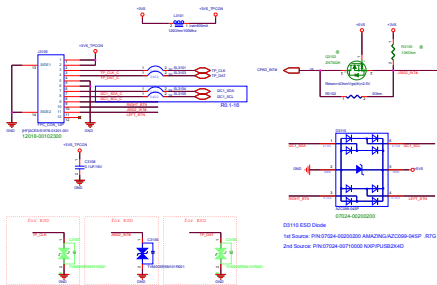
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To Touchpad

To Touchpad Buffer



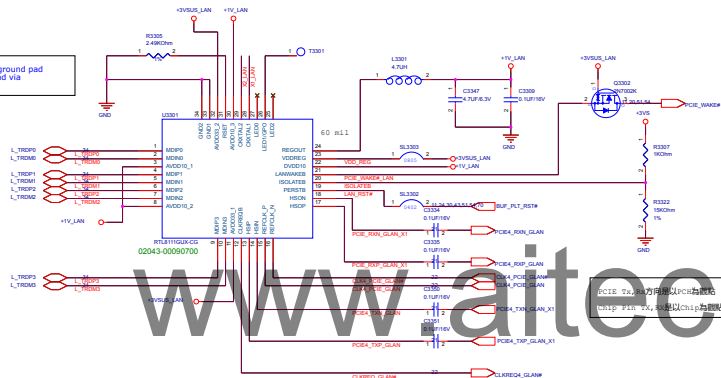


The top diagram shows the main power supply and a 3.3V regulator. The bottom diagram shows a 3.3V regulator and a 1.8V regulator. Both diagrams include component values and pin connections.

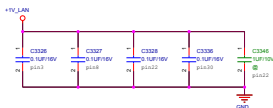
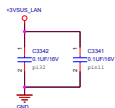
Main Board

The distance from U3301.24 to L3301 within 200 mil.  
The distance from L3301 to C3347 within 200 mil.

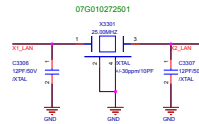
33/34 pin ground pad  
need ground via



CLKREQ\_GLAN#, PCIE\_WAKE#  
should be PU on the host side

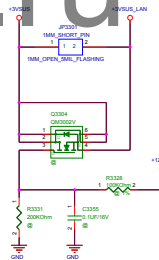


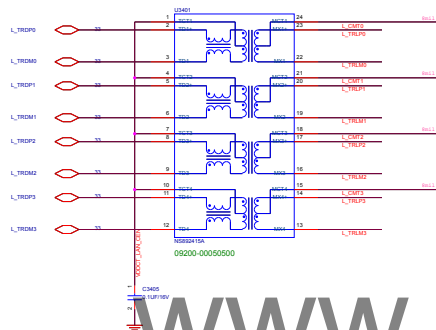
C3348, C3310 close to pin 23 reserved for SWR mode



X3301: 25MHZ +/-30ppm/10pF (3225)  
1st: P/N:07G010272501 TXC/7V2500001 1  
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V\_LAN raise time >1ms





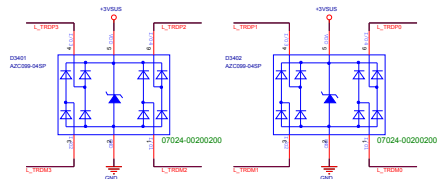
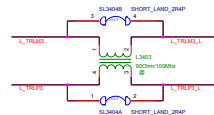
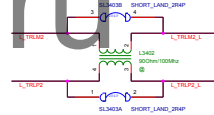
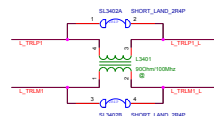
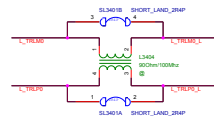
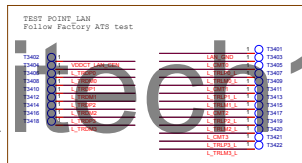
## LAN Connector



J3402 LAN Jack

1st Source: P/N:12014-00161700 FOXCONN/JM361 1-NS640003-7H

2nd Source: P/N:12014-00035500 SINGA TRON/2RJ1648-000111F



D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP .R7G

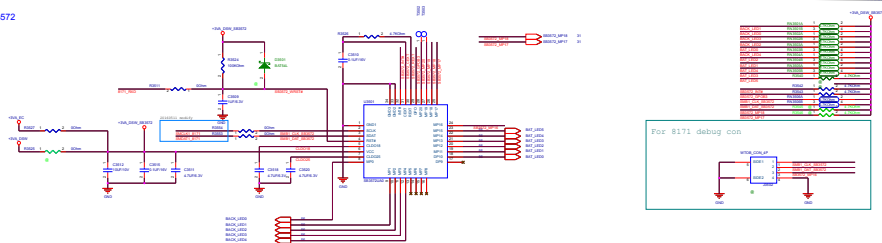
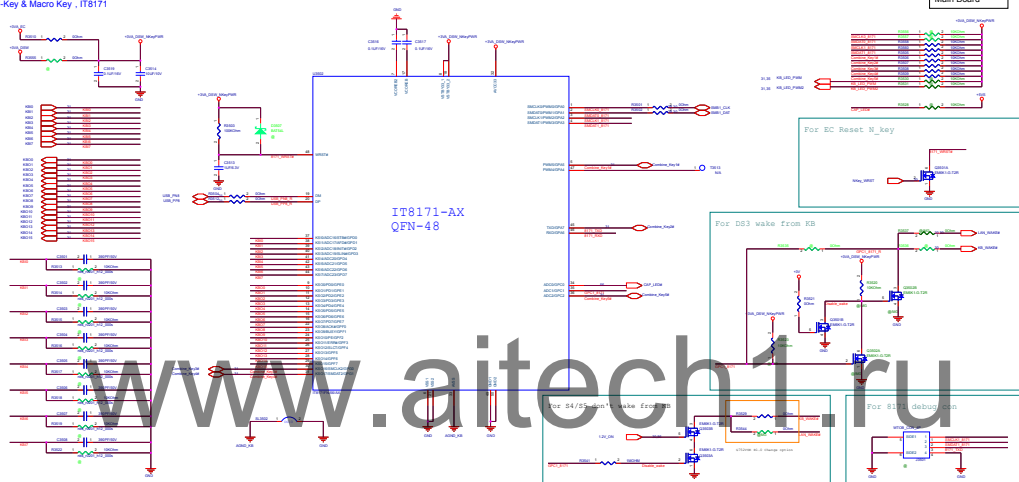
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

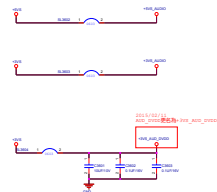
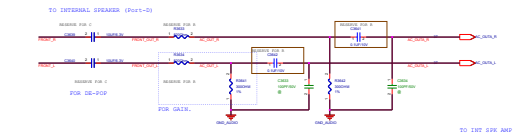
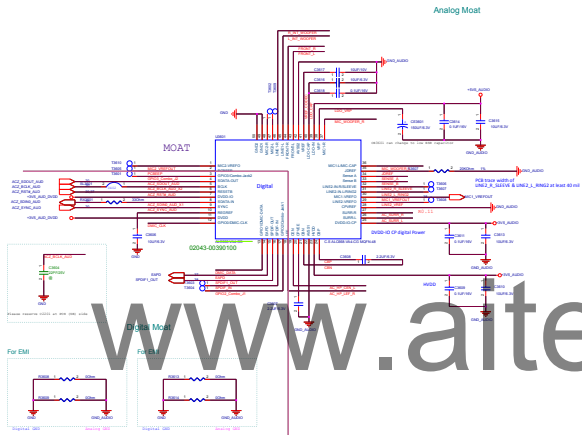


2012/2/16 EMI



Place near chassis GND



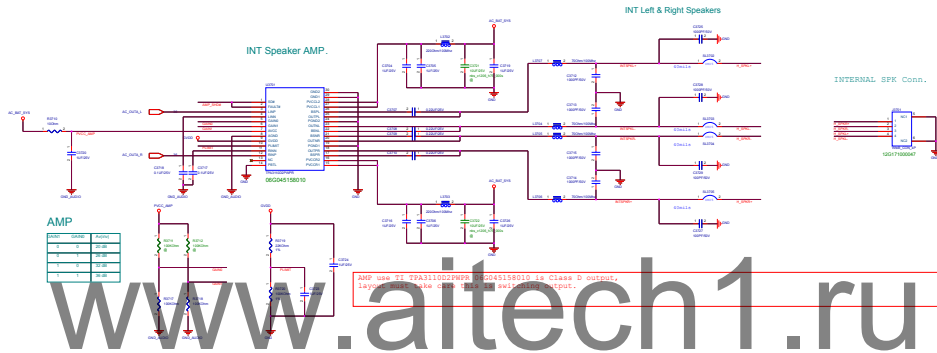


## DETECTION

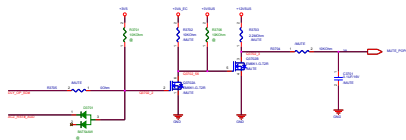


Design IF Hi-F. Item 10. Place route number AND length as NUMBER IN AC 1  
like differential signal. It is to avoid self-interference. Place these components near coded side.

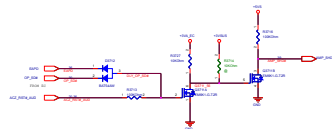




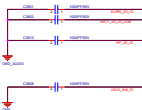
EXT JACK MUTE CONTROL



INT SPK MUTE CONTROL



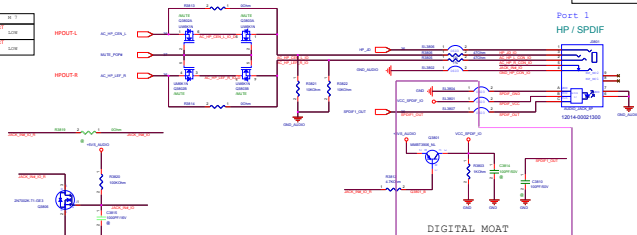
For EMI



HP & SPDIF DETECT RULE

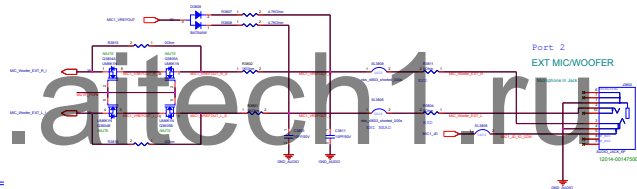
	IN 5	IN 4	IN 3
HPDET_HIP	LOW	LOW	LOW
HPDET_SPD	LOW	LOW	LOW
HPDET_HIPDET	LOW	LOW	LOW

For EMI



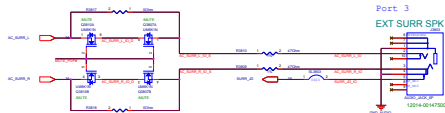
2013/01/18 NAKSOLUR  
Fix HP PDP Noise Issue in Resume S3  
Change Power plan from <S3> to <S4>

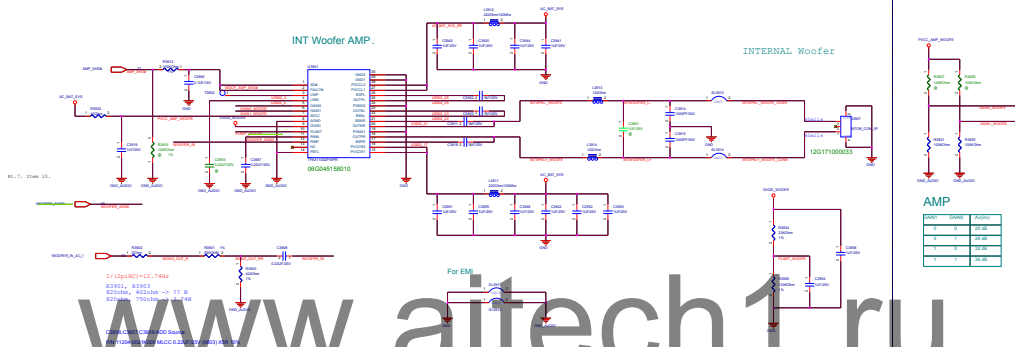
For EMI



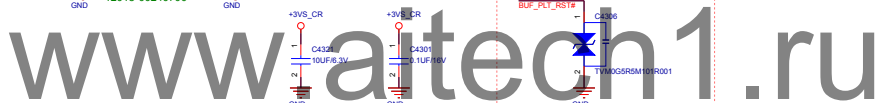
2013/01/18 NAKSOLUR  
Fix HP PDP Noise Issue in Resume S3  
Change Power plan from <S3> to <S4>

For EMI





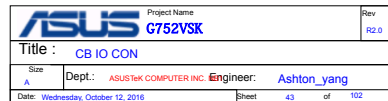




## CardReader PWR



For EMI



## LPC Debug Port



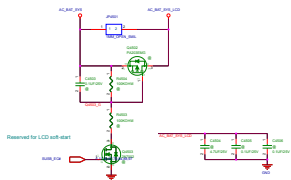
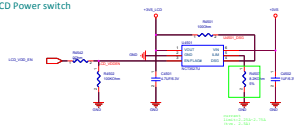
JDEB4401 Connector (MP USE)

1st Source: P/N:12018-00102300 ACES/51578-01201-001

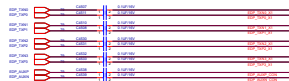
2nd Source: P/N:12018-00102400 ENTER Y/6705K-Y12N-00L

<b>ASUS</b>		Project Name	Rev
<b>G752VSK</b>			R2.0
Title: <b>BUG NewCard &amp; LPC</b>			
Size	Dept.:	Engineer:	
A	ASUSTek COMPUTER INC.	Ashton_yang	
Date: Wednesday, October 12, 2016	Sheet	44	of 102

# LCD Power switch



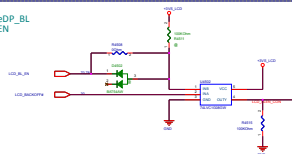
# eDP circuit



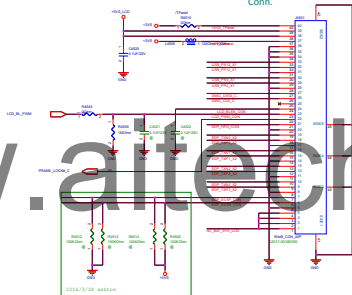
# eDP\_HPD



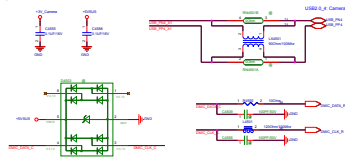
# eDP\_BL EN



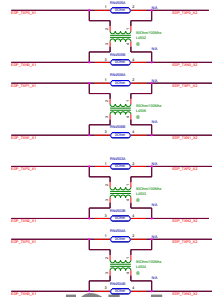
# eDP Panel Conn.



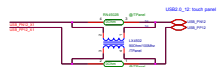
# Camera & D-MIC



# For EMI

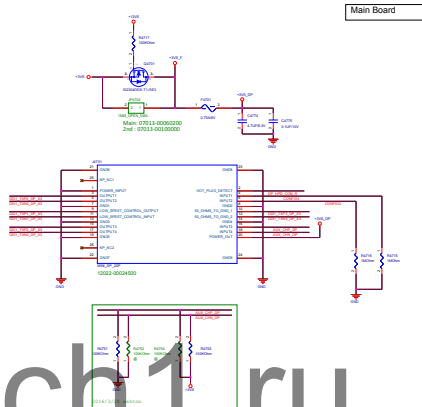
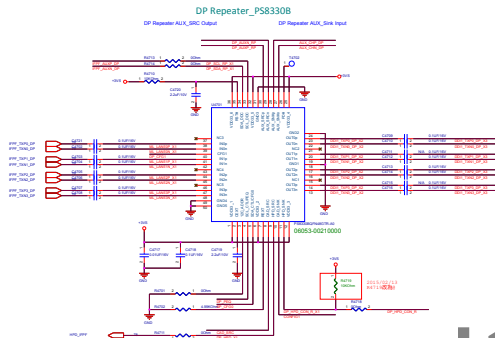


# Touch Panel



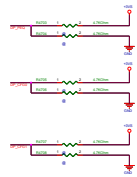
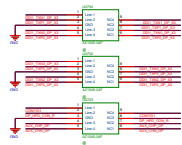
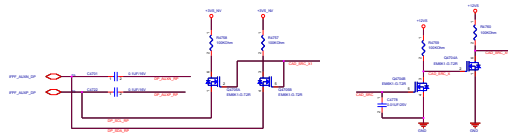
Main Board

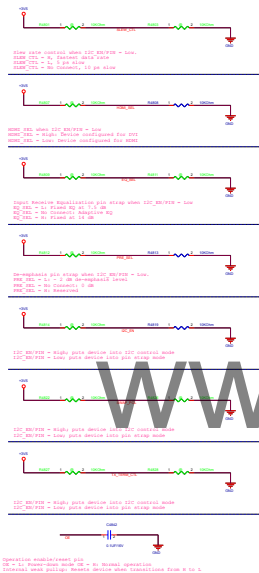
www.aitech1.ru



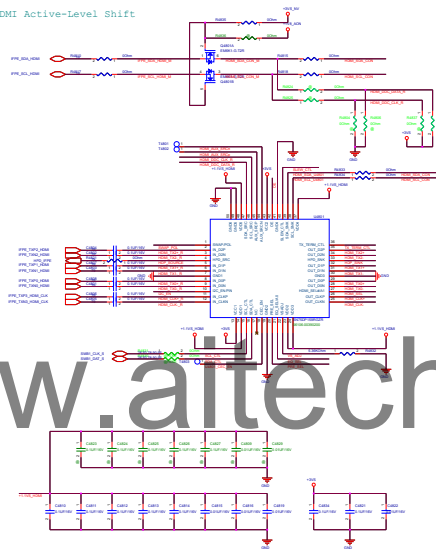
www.aitech1.ru

2014/3/28  
 BULTR000 Rev.0.00 reference Pinade Design Circuit PS8330B  
 Pin MUX2P To MUX2 Single No Display Issue

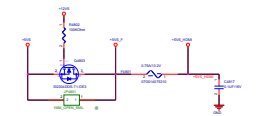




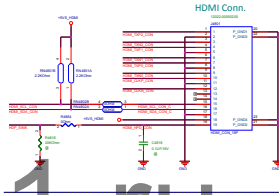
## HDMI Active-Level Shift



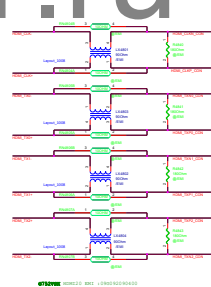
## HDMI PWR\_+5VS\_HDMI



## HDMI Conn.



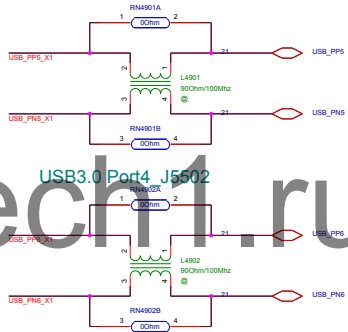
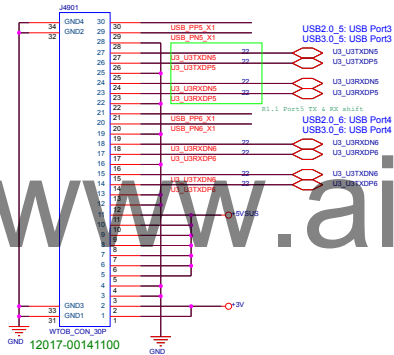
## HDMI EMI



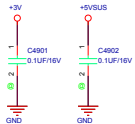
Main Board

To USB3.0 I/O Board (PAGE55)

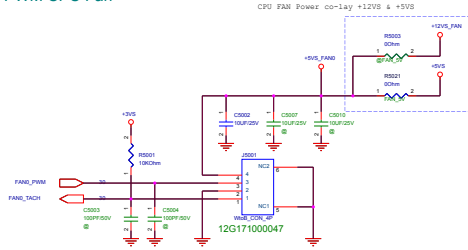
USB3.0 Port3\_J5501



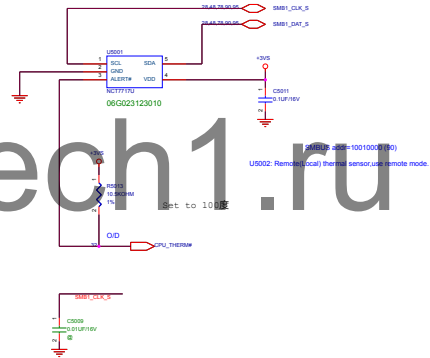
USB3.0 Port4\_J5502



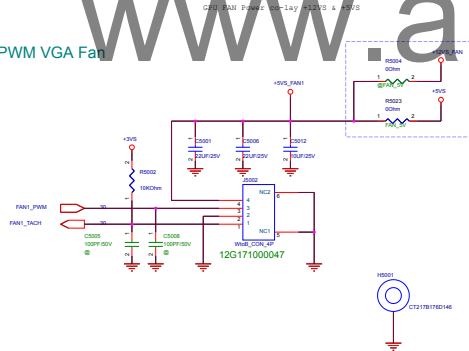
## PWM CPU Fan

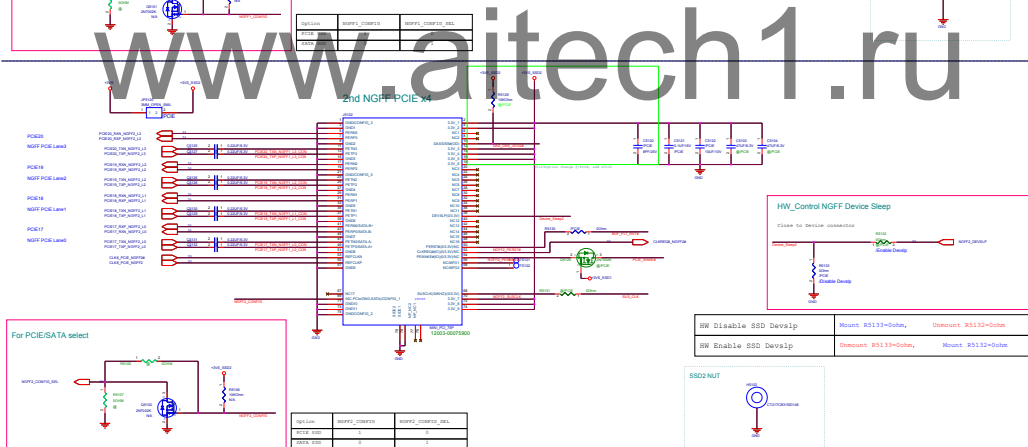
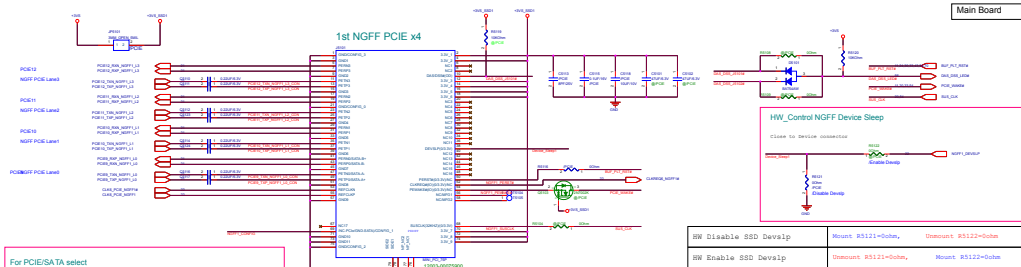


## CPU Thermal Sensor



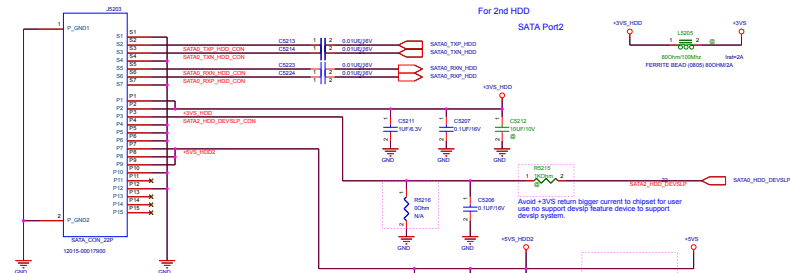
## PWM VGA Fan







## 2nd HDD



## EMI Request



1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

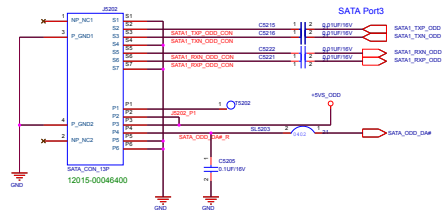
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

## For RF requirement

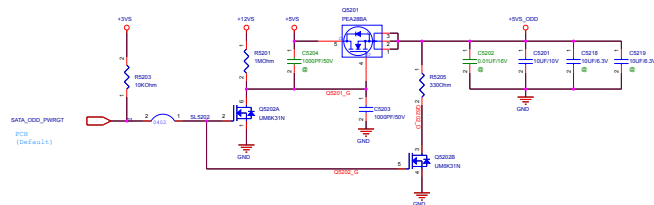
EMI Request0520



## ODD



## ODD Power



## Main Board



--

## USB3.0 ESD-Protection



## USB2.0 ESD-Protection



2nd Source: P/N:07024-00710000 NXP/PU5B2X4D

10. *Journal of the American Medical Association*, 2000; 284: 2561-2566.



2nd Source: PIN:07034-00710000 NXP/PU5B2X4D

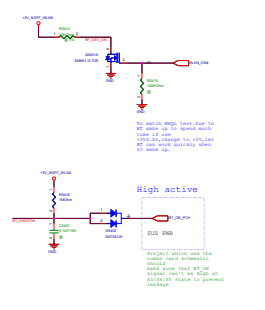
10. *Journal of the American Medical Association*, 2000; 284: 2689-2694.

```
NGFF M.2 TYPE_E-KEY WIFI
```



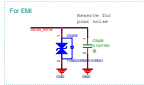
76	RESEARCH	RESEARCH	76
77	RESEARCH	RESEARCH	77
78	RESEARCH	RESEARCH	78
79	RESEARCH	RESEARCH	79
80	RESEARCH	RESEARCH	80
81	RESEARCH	RESEARCH	81
82	RESEARCH	RESEARCH	82
83	RESEARCH	RESEARCH	83
84	RESEARCH	RESEARCH	84
85	RESEARCH	RESEARCH	85
86	RESEARCH	RESEARCH	86
87	RESEARCH	RESEARCH	87
88	RESEARCH	RESEARCH	88
89	RESEARCH	RESEARCH	89
90	RESEARCH	RESEARCH	90
91	RESEARCH	RESEARCH	91
92	RESEARCH	RESEARCH	92
93	RESEARCH	RESEARCH	93
94	RESEARCH	RESEARCH	94
95	RESEARCH	RESEARCH	95
96	RESEARCH	RESEARCH	96
97	RESEARCH	RESEARCH	97
98	RESEARCH	RESEARCH	98
99	RESEARCH	RESEARCH	99
100	RESEARCH	RESEARCH	100

## WLAN &amp; BT ON



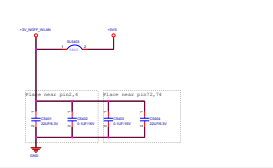
**WLAN NUT**

HWADDR: 08:00:27:00:00:00  
EUI-64: 02:00:00:00:00:00:08:00  
MAC-Address: 08:00:27:00:00:00  
Name: wlan\_nut\_0000

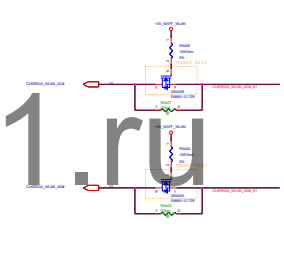
[illegible]

## Main Board

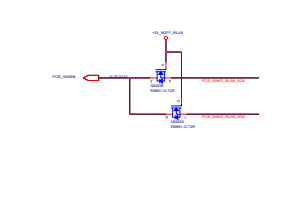
WLAN PWR\_+3V\_NGFF\_WLAN  
(Non-ISCT)



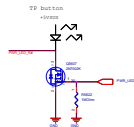
## WLAN CLKREQ#

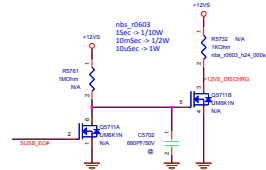


## WLAN\_Wake# Control

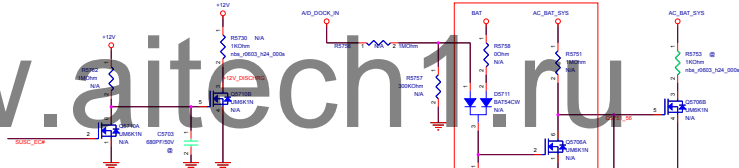


## Main Board

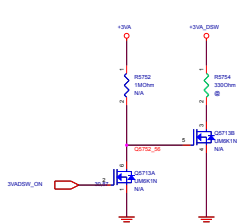
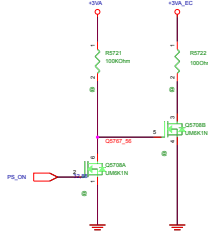
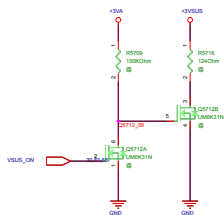




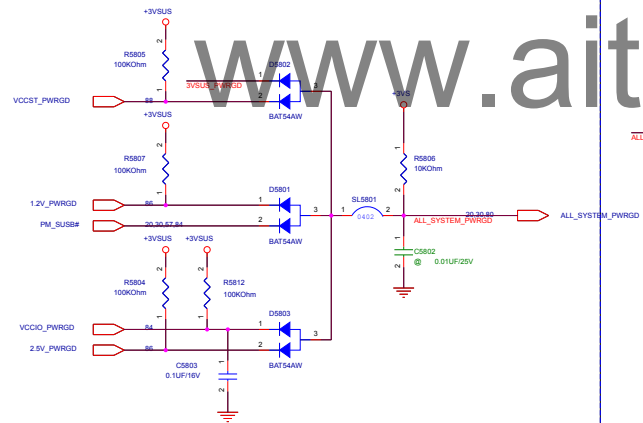
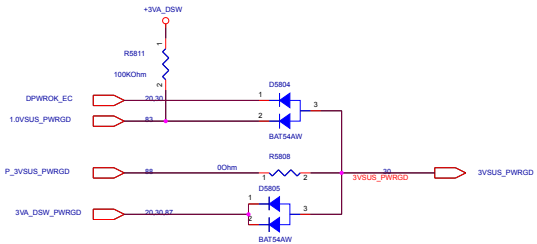
SUSC\_EC# turn off discharge before +12V ON  
+12V turn on discharge after SUSC\_EC# OFF



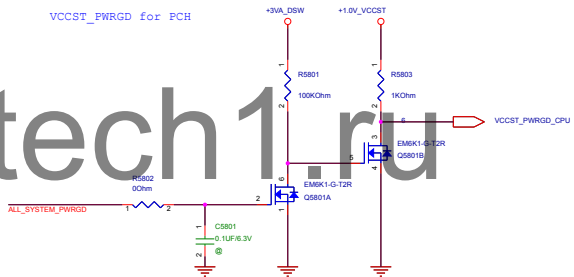
每小時耗 0.45mW  
每個月耗 324mW  
 $0.45\text{mW} = (15 \times 15 / 1\text{M}) \times 2$



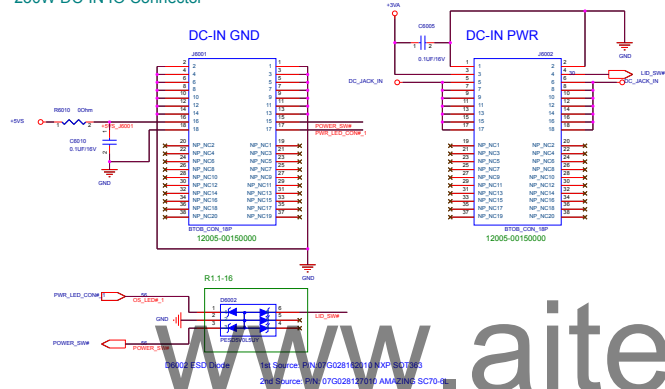
Main Board



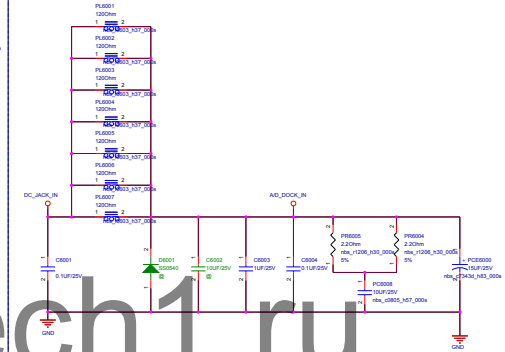
VCCST\_PWRGD for PCH



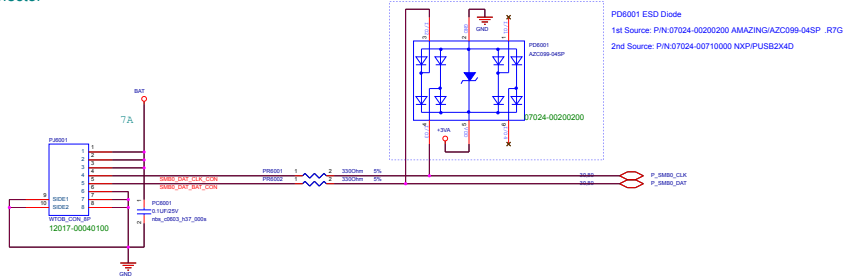
## 230W DC-IN IO Connector



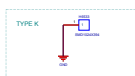
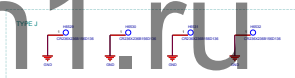
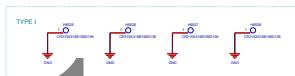
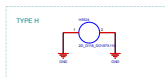
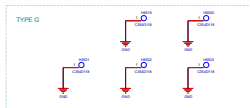
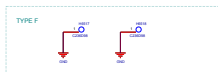
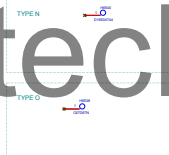
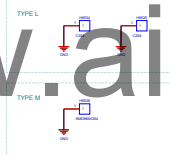
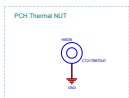
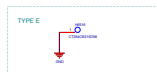
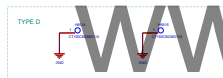
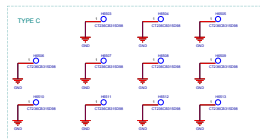
## Main Board



## Battery Connector



## TOP Component



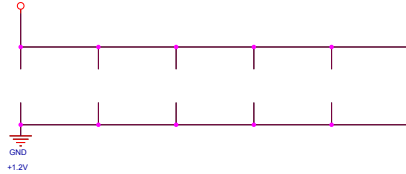
Main Board

## BOT Component

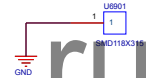
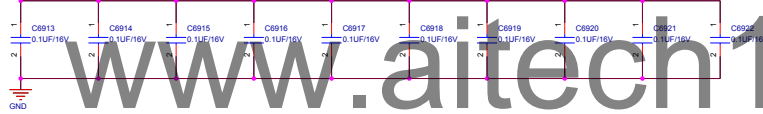
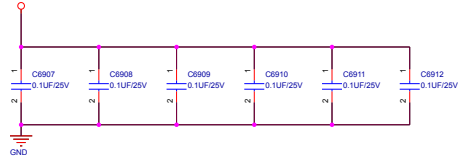


EMI

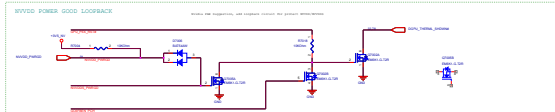
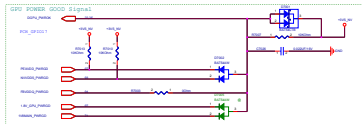
G\_PWR\_SRC\_NVVDD



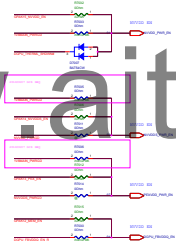
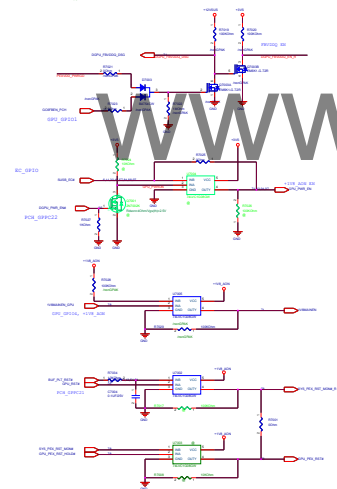
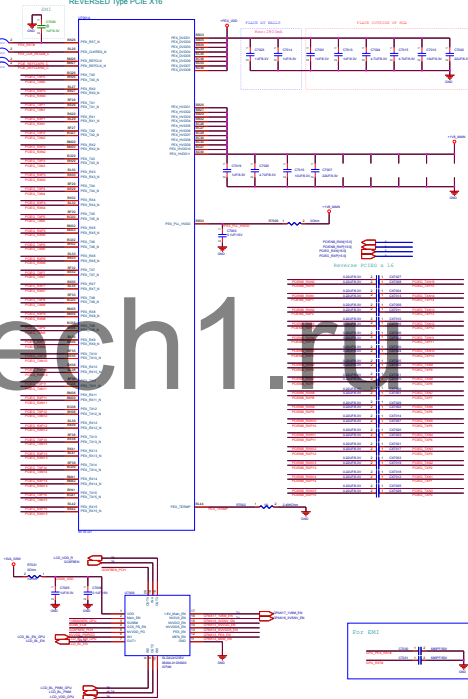
P\_IMVP8\_VCORE\_VIN\_S

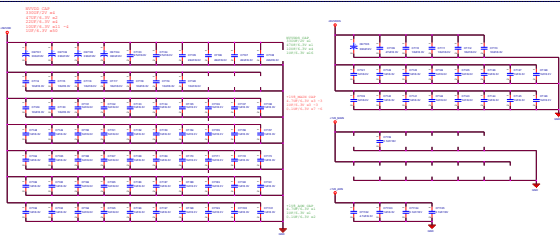
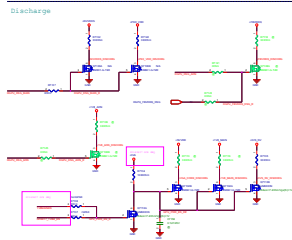
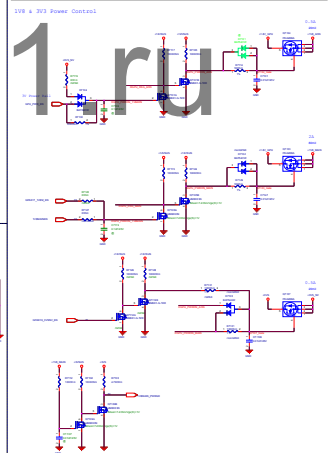
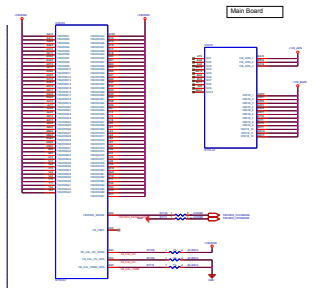
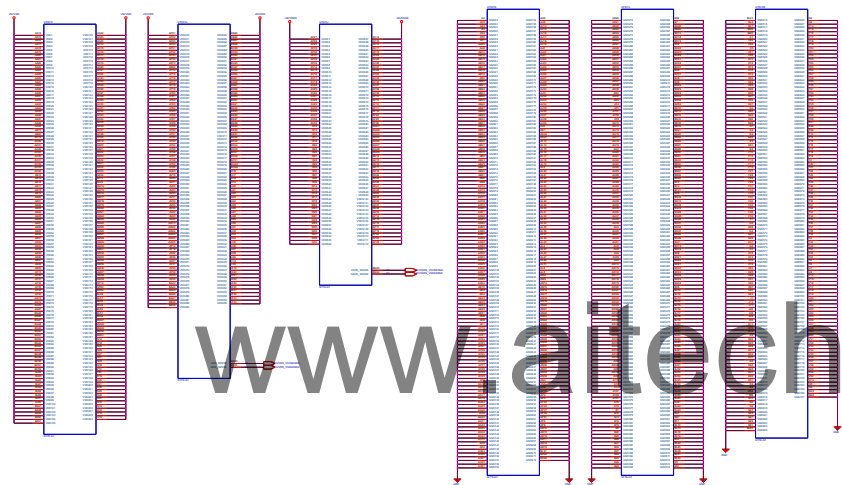


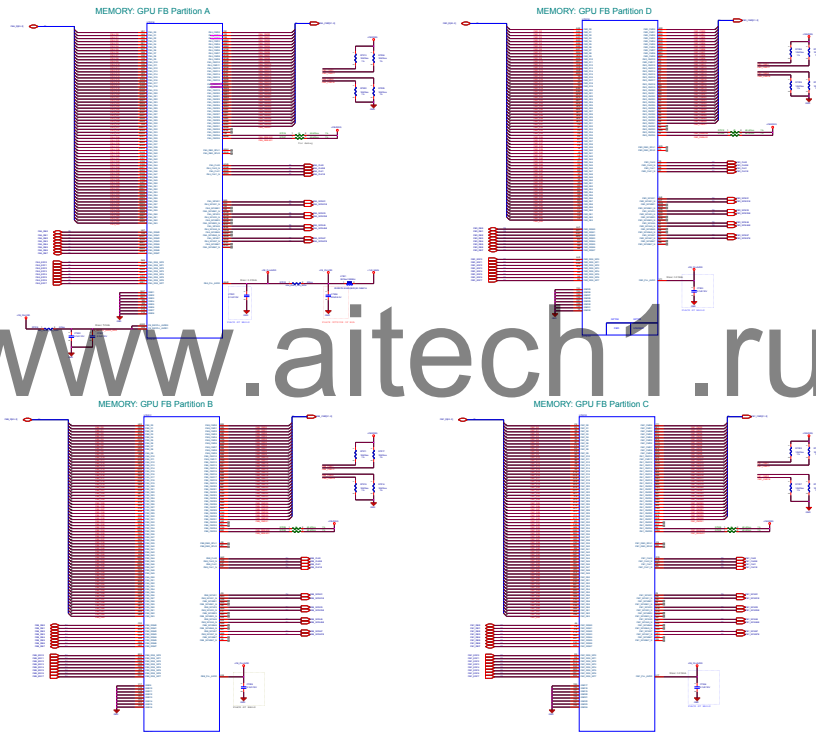
www.aitech1.ru



## GPU POWER SEQUENCE CONTROL

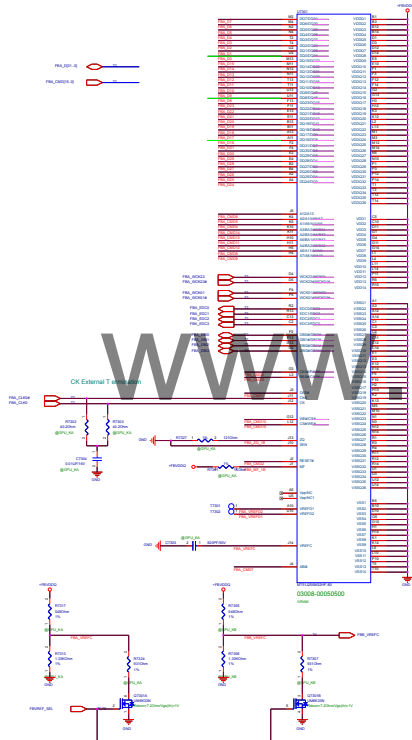
PCI EXPRESS\_Graphics  
REVERSED 3-- PCI-E X16





# FBA Partition Memory (1 of 2)

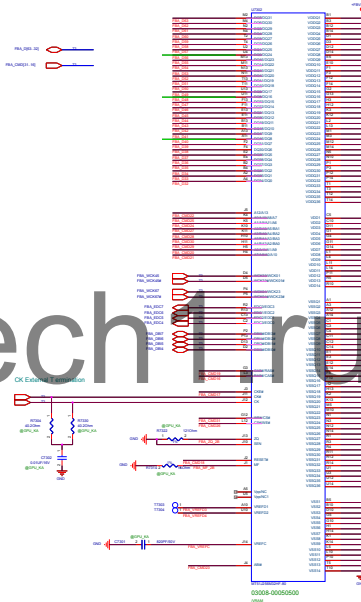
MF=1 Mirror



# FBA Partition Memory (2 of 2)

Main Board

MF=0 Normal



01 3-02 01 2-02

USE GDD55 VGRAM (2880 x 32 (512MB))

1st: PIN 03008-00030100 HYUNDAI HYNIX H5GC41Q4MFR T2C (M-dw) .Step: 0 x2

2nd: PIN 03008-00030205 SAMSUNG K4132DFC-HC33 .Step: 0x3

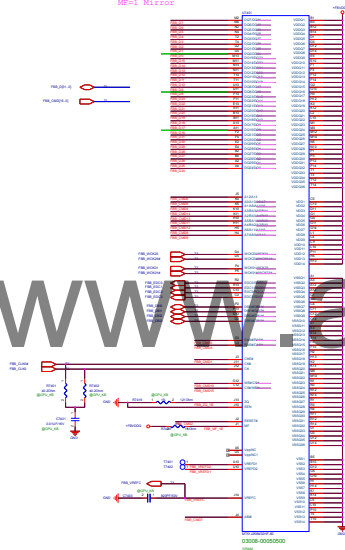
3rd: PIN 03008-00030400 Micron EDW532BAG-60 F (B-dw) .Step: 0x4

GDD5 MODE SELECTION

MODE	MF	SW1	SW2
00	0	VDD	VDD
01	1	VDD	VDD
02	0	VDD	VDD
03	1	VDD	VDD

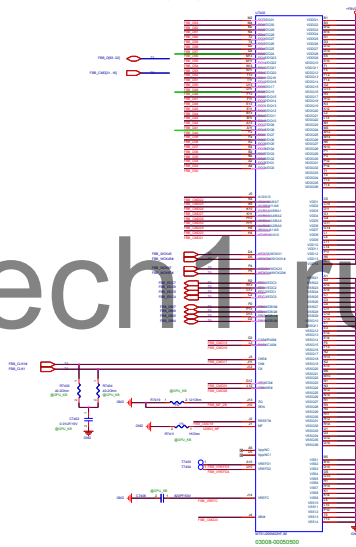
# FBB Partition Memory (1 of 2)

MF=1 Mirror



# FBB Partition Memory (2 of 2)

MF=0 Normal



03008-00000000

03008-00000000

03008-00000000

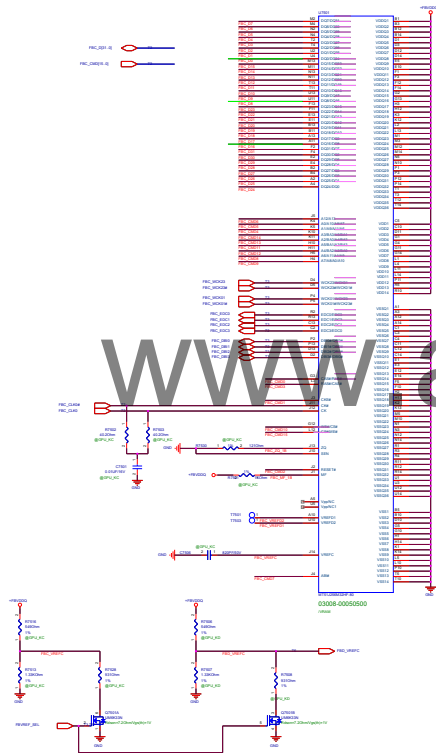
## GDD5 MODE SELECTION

MODE	MF	MODE	MODE
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3

Main Board

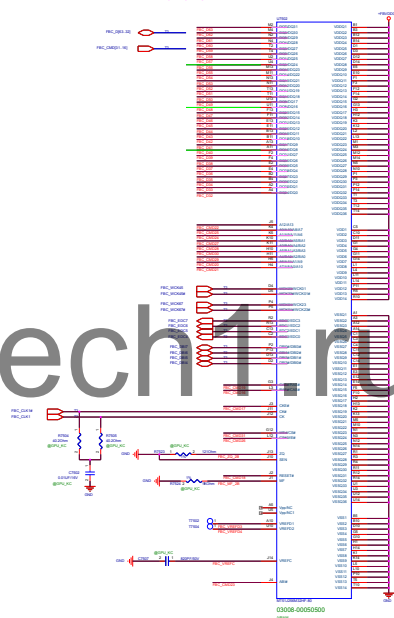
# FBC Partition Memory (1 of 2)

MF=1 Mirror



# FBC Partition Memory (2 of 2)

MF=0 Normal



PH 3-00 PH 2-05

USE GDDR5 VRAM (2GB x 32 (128MB))

1st PIN 03008-00030100 HYUNDAI H5GQ4H4MTR-T2C (M-die) (Strap 0 x2)

2nd PIN 03008-00030200 SAMSUNG K4G4132PFC HCCS (Strap 0x3)

3rd PIN 03008-00030400 Micron EDV4932BAG-60-F (B-die) (Strap 0x4)

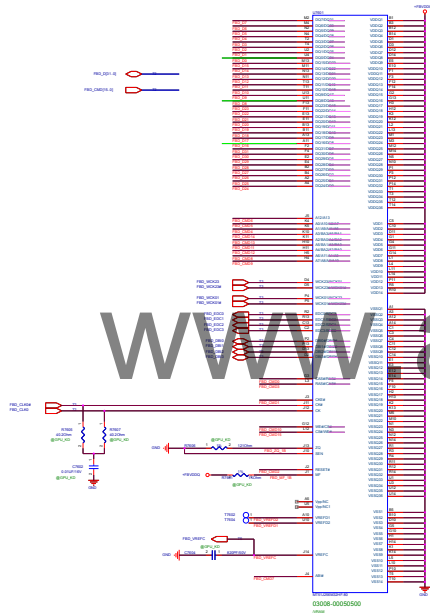
## GDDR5 MODE SELECTION

MODE	MF	MODE	MODE
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
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91	91	91	91
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93	93	93	93
94	94	94	94
95	95	95	95
96	96	96	96
97	97	97	97
98	98	98	98
99	99	99	99

Main Board

## FBD Partition Memory (1 of 2)

MF=1 Mirror

03008-00050500  
/v/f/2021/

**R1.3-02**   **R1.2-25**

USE GDDR5 VRAM (288Mb x 32 (512MB))

1st: P/N:03008-00030100 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

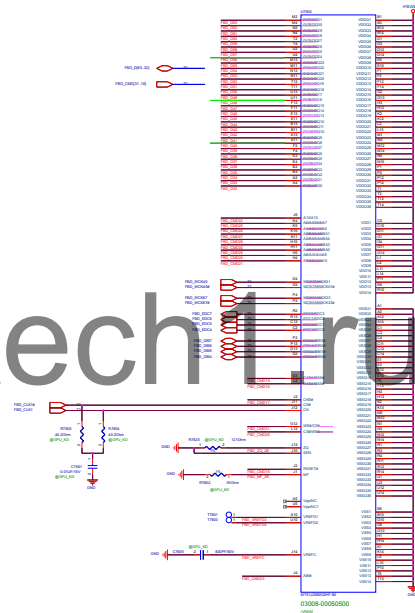
3rd: P/N 03008-00030400 Micron/EDW4032BAG-60-F (B-die) ,Strap: Oxide

## GDD5 MODE SELECTION

Model	df	SS	MS
1	1	1	1.000
2	1	1.000	1.000
3	1	1.000	1.000
4	1	1.000	1.000

## FBD Partition Memory (2 of 2)

MF=0 Normal

03008-0005050  
05AM

**R1.3-02**   **R1.2-25**

USE GDDR5 VRAM (288Mb x 32 (512MB))

1st: P/N:03008-00030100 HYNIXH5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

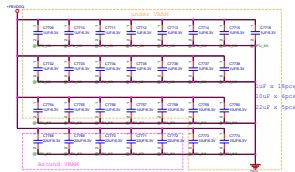
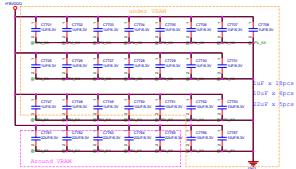
3rd: P/N 03008-00030400 Micron/EDW4032BAG-60-F (B-die) ,Strap: Oxide

## GDD5 MODE SELECTION

Model	df	SS	MS
1	1	1	1.000
2	1	1.000	1.000
3	1	1.000	1.000
4	1	1.000	1.000



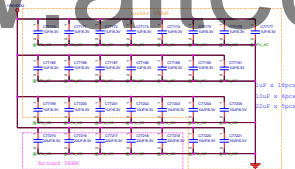
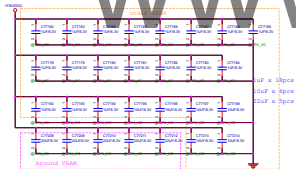
Channel A



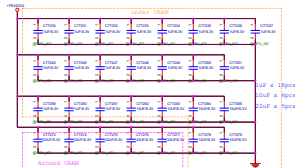
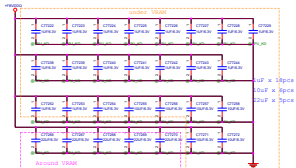
Channel B



Channel C

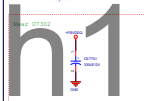
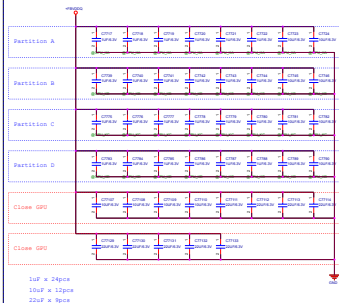


Channel D



VRAM\_FWR\_FBVDQ

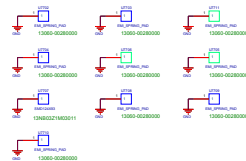
Main Board



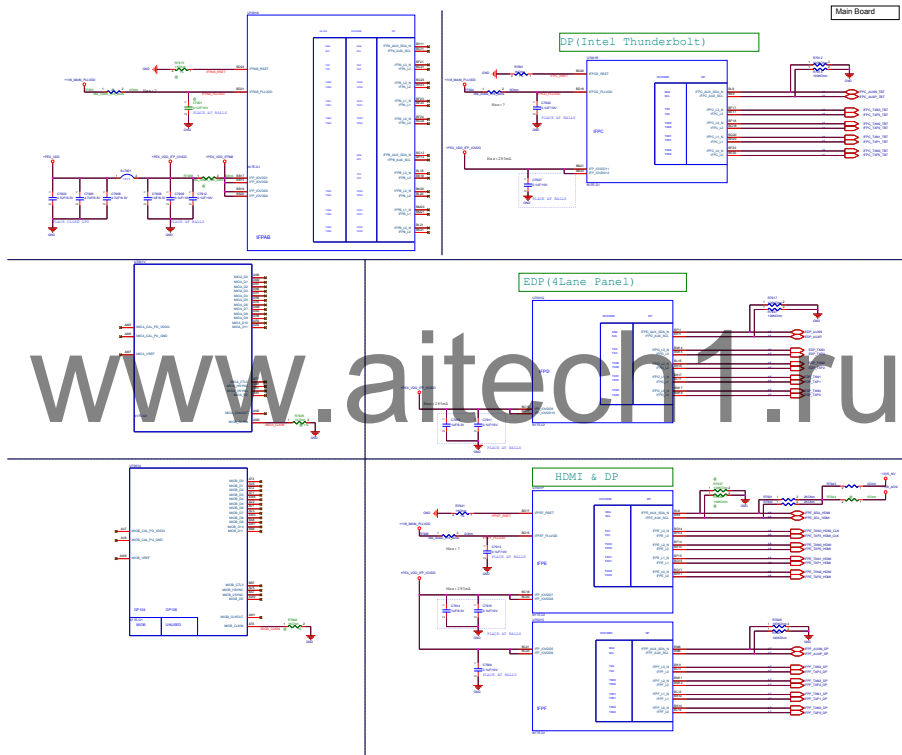
DGPU EMI GND Pad

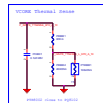
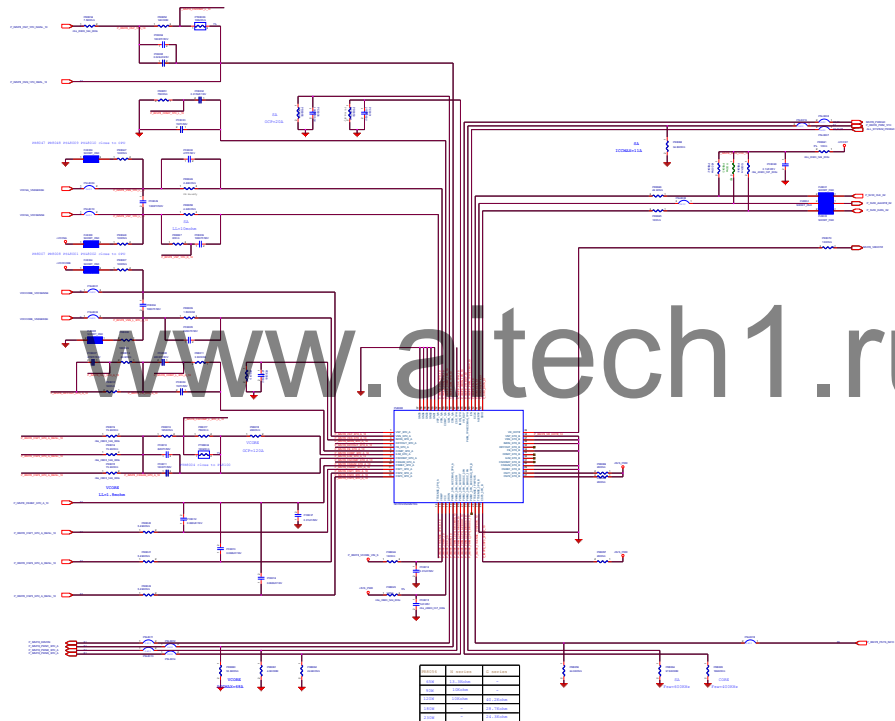
EMI

EMI DGPU Spring

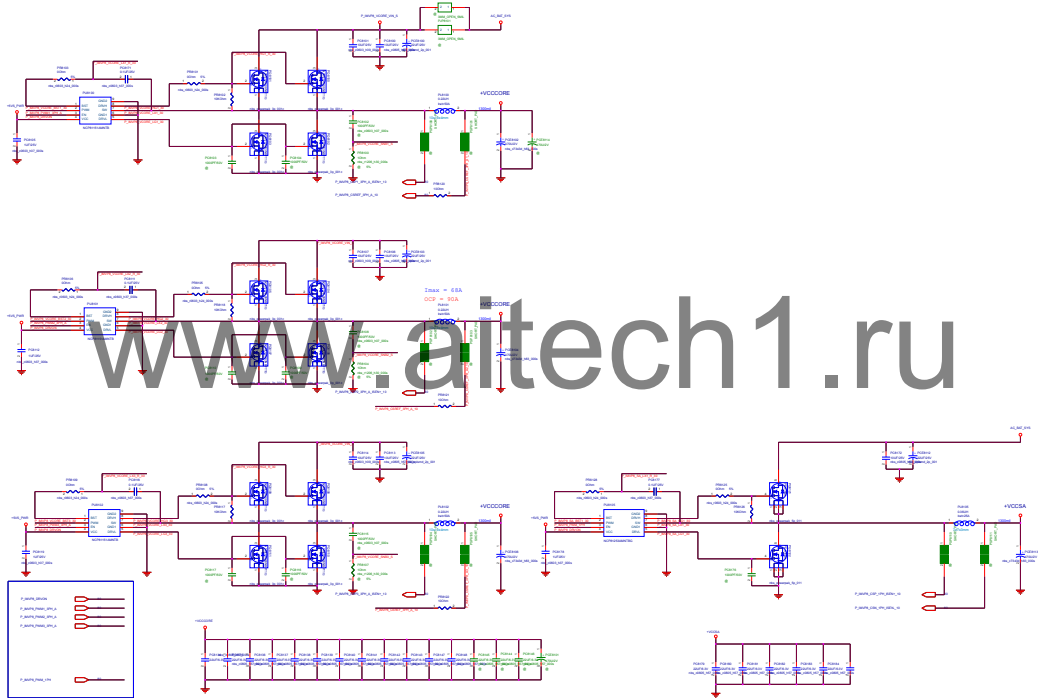




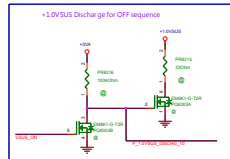
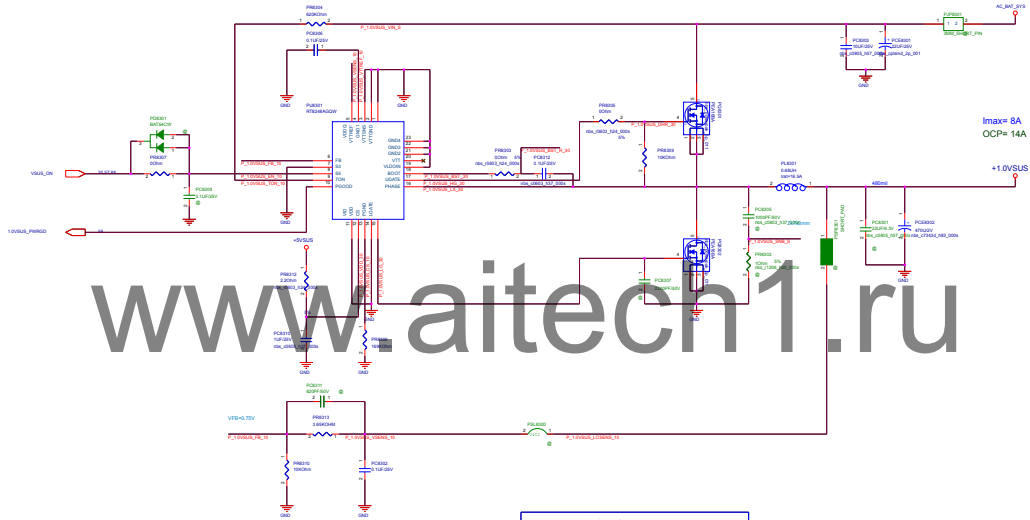




# SkyLake IMVP8 Power (For CPU)



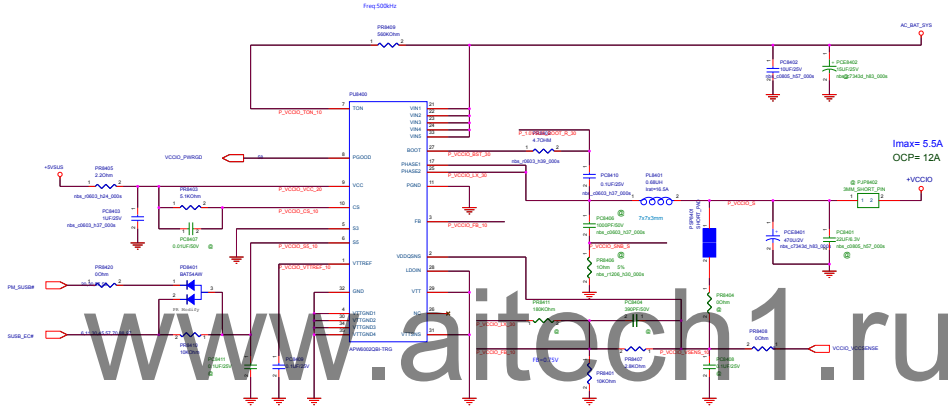
+1.0VSUS [For PCH]



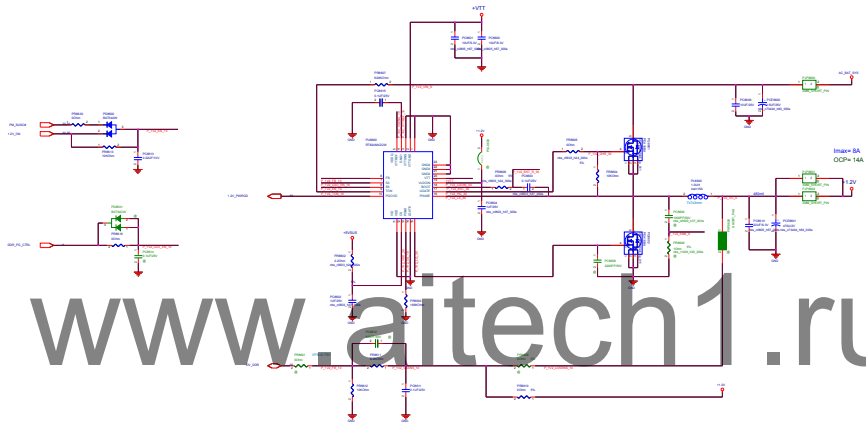
©Gee Design

ASUS		Project Name	Rev
Title : PW_+1.0VSUS			Rev 6
Size	Dept: A8 Power team	Engineer: Benson	
Date: November 04, 2014	Print: 81	of 100	

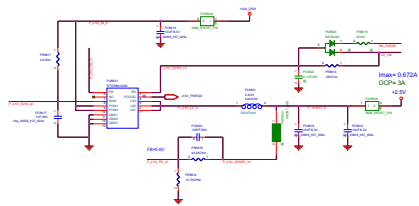
*+VCCIO [For CPU]*



+1.2V / VTT / 2.5V[For Memory]

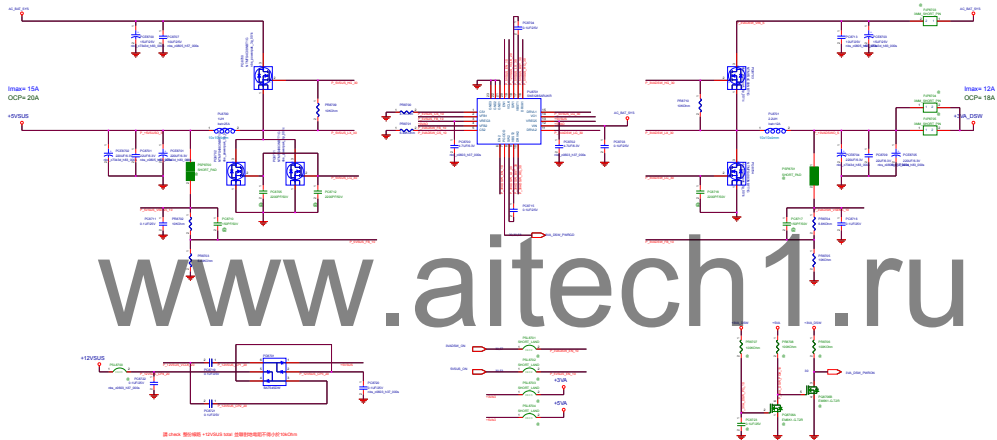


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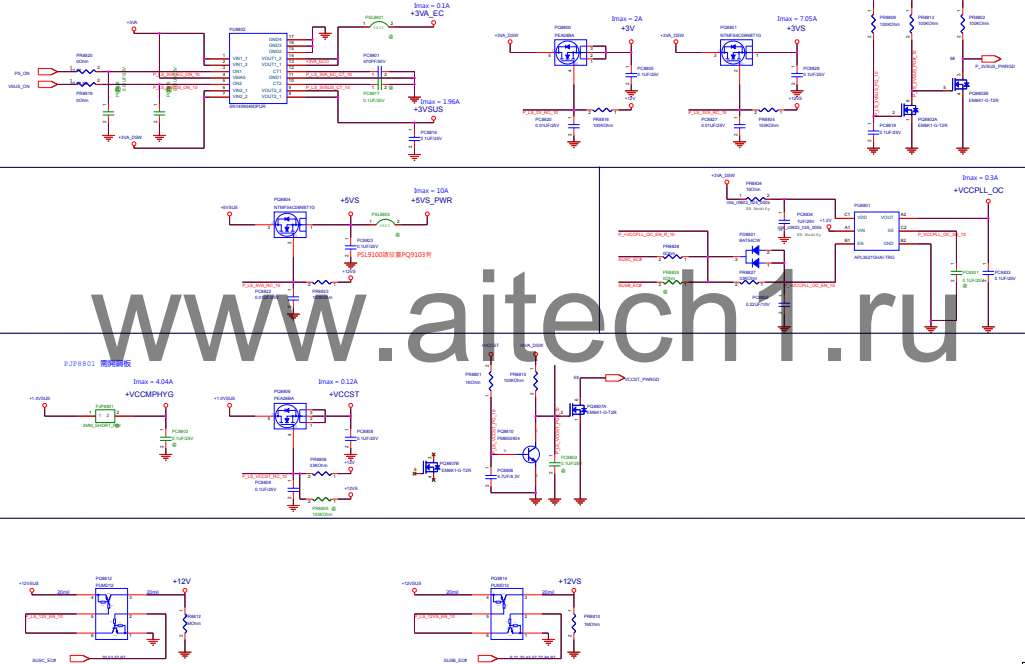
+3VA\_DSW / +5VSUS [System Power]



Output Voltage (mVrms)

	80	108	83	103	84	85	86 with USB Charger
PIN_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
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SWINGING_ON	1	-	1	-	1	-	1
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SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON	1	-	1	-	1	-	1
SWINGING_ON							

# Load Switch





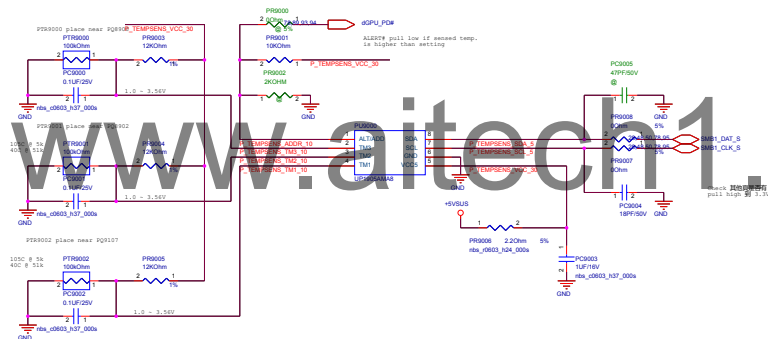
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
999001	10%	1.5%	2%	3.6%	1.9%	4.3%	5.1%	6%
999002	Open	8.2%	6.2%	6.8%	4.7%	3.6%	2.7%	2%

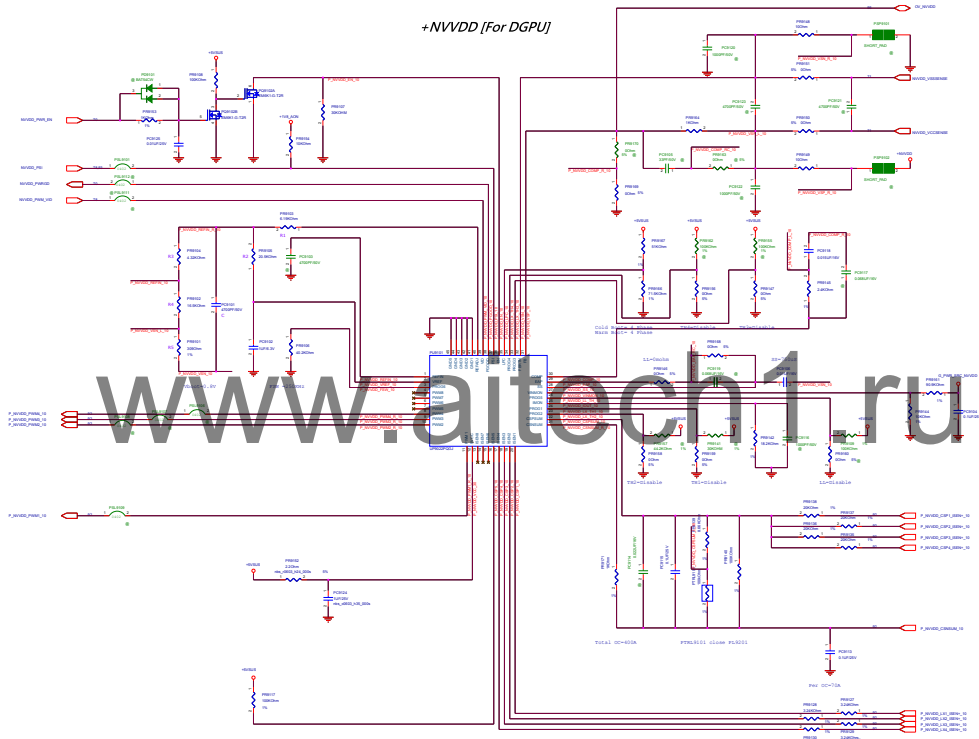
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

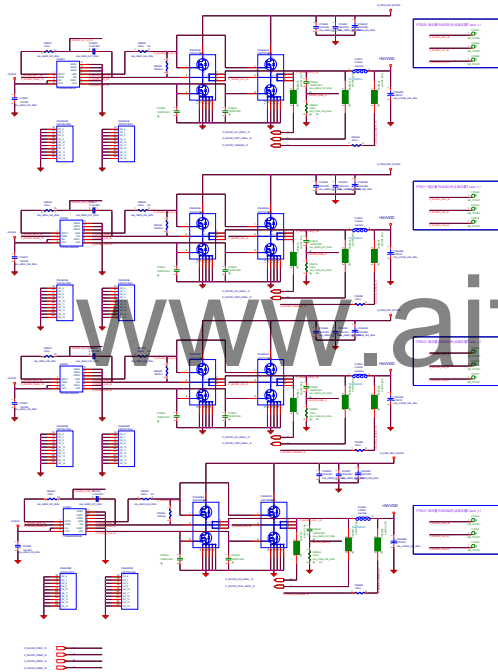
Main Board



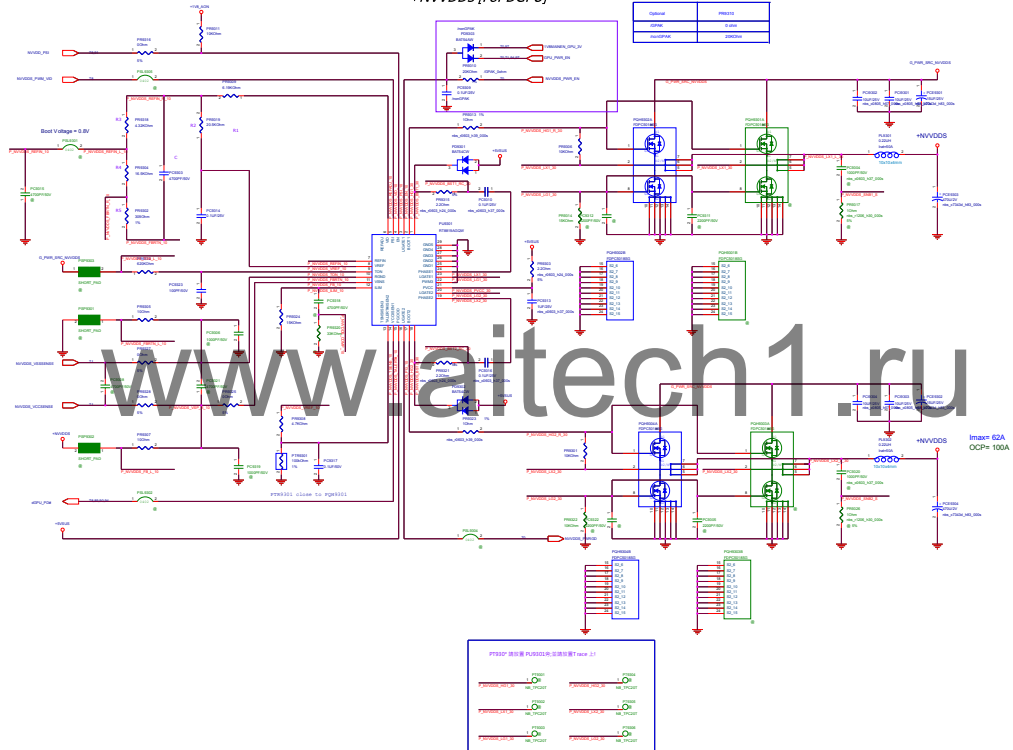
+NVVDD [For DGPU]



+NVVDD [For DGPU]

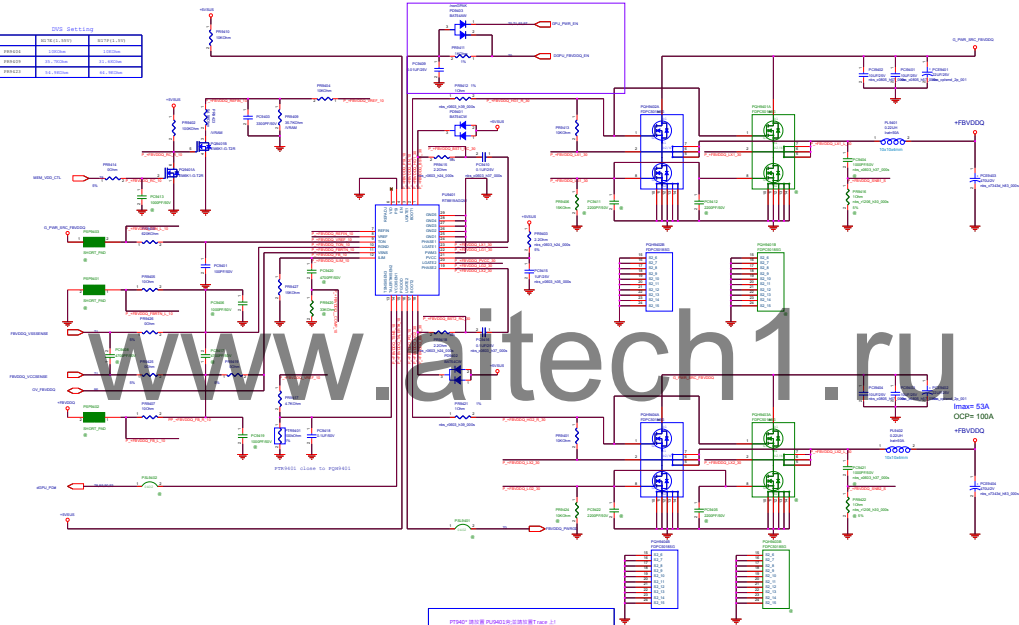


Cytosol	PRK310
IGF1R	0.0000
nonIGF1R	2000000



+FBVDDQ [For VRAM]

DQS Setting	
DS1E(L1,DS1)	DS1F(L1,DS1)
DS2E(L1,DS2)	DS2F(L1,DS2)
DS3E(L1,DS3)	DS3F(L1,DS3)
DS4E(L1,DS4)	DS4F(L1,DS4)
DS5E(L1,DS5)	DS5F(L1,DS5)
DS6E(L1,DS6)	DS6F(L1,DS6)
DS7E(L1,DS7)	DS7F(L1,DS7)
DS8E(L1,DS8)	DS8F(L1,DS8)
DS9E(L1,DS9)	DS9F(L1,DS9)
DS10E(L1,DS10)	DS10F(L1,DS10)
DS11E(L1,DS11)	DS11F(L1,DS11)
DS12E(L1,DS12)	DS12F(L1,DS12)



PWR000 電源線 PWR000 電源線	
PWR000_000	PWR000_000
PWR000_001	PWR000_001
PWR000_002	PWR000_002
PWR000_003	PWR000_003
PWR000_004	PWR000_004
PWR000_005	PWR000_005
PWR000_006	PWR000_006
PWR000_007	PWR000_007
PWR000_008	PWR000_008
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PWR000_100	PWR000_100

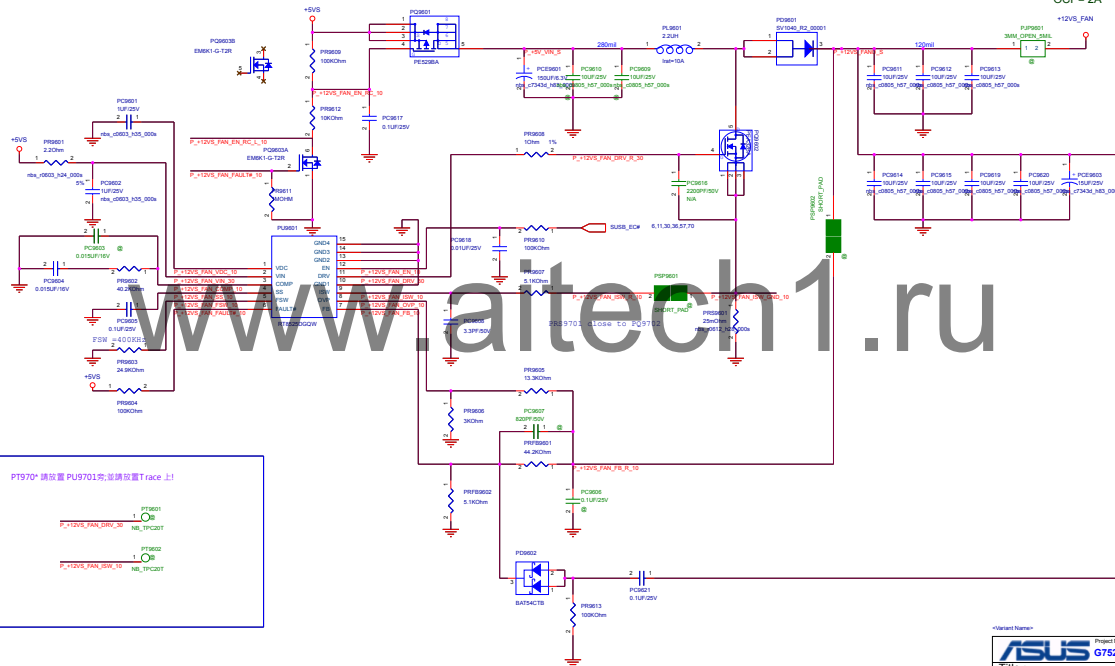




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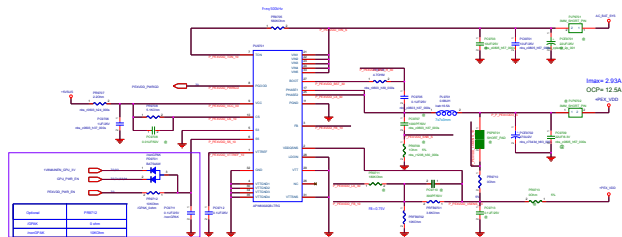
OCP = 2A

+12V<sub>S\_FAN</sub>



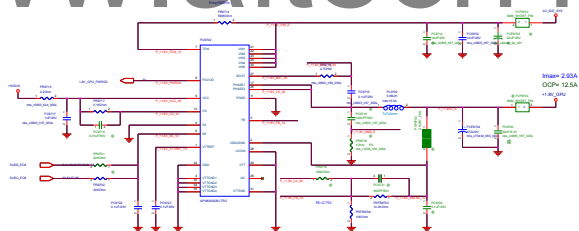
<Variant Name>

ASUS		Project Name	Rev
G752VSK			B2.0
Title : PW_+12VS_FAN			
Size	Dept.:	NO Power team	Engineer: Benson
Date: Wednesday, October 13, 2016		Sheet	95 of 102

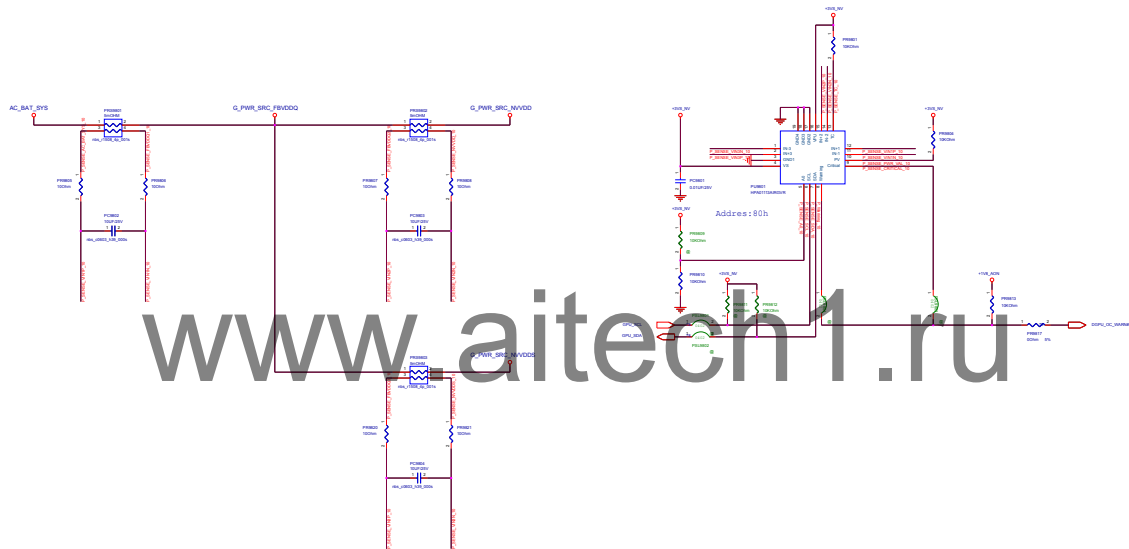


VRM1	VRM1
VRM2	VRM2
VRM3	VRM3
VRM4	VRM4

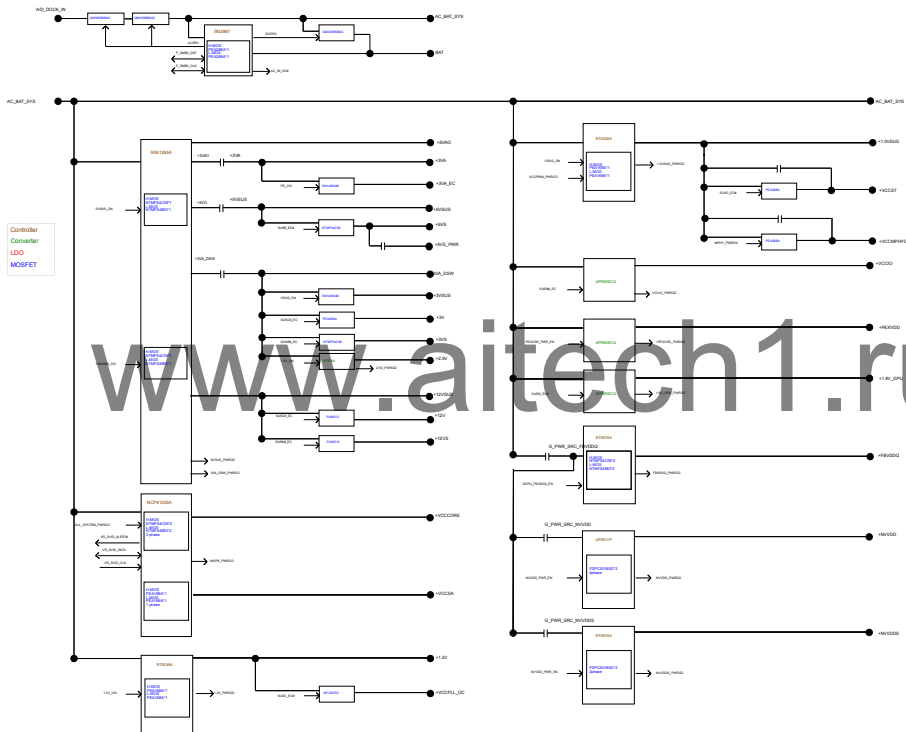
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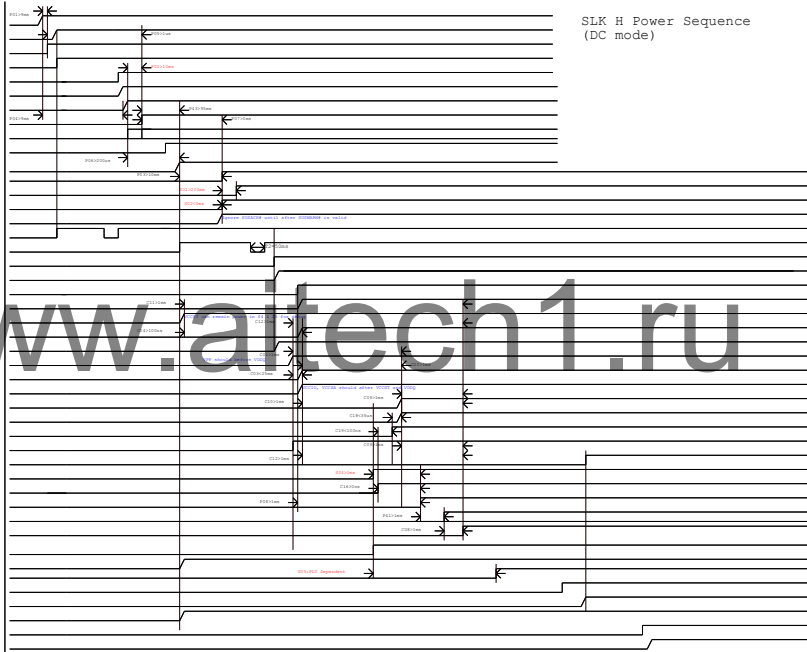
VRM1	VRM1
VRM2	VRM2
VRM3	VRM3
VRM4	VRM4



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[illegible]SLK H Power Sequence  
(DC mode)